Department of Electrical & Electronics Engineering

Course File

ADVANCED POWER ELECTRONIC CONVERTERS

(Course Code: GR20D5037)

I M.Tech II Semester

2021-22

Dr. Suresh Kumar Tummala
Professor

Gokaraju Rangaraju Institute of Engineering & Technology
(Autonomous)
Bachupally, Kukatpally, Hyderabad – 500 090, A.P., India.

ADVANCED POWER ELECTRONIC CONVERTERS

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Gokaraju Rangaraju Institute of Engineering and Technology
(Autonomous)

Department of Electrical & Electronics Engineering

Int. Marks:30 Ext. Marks:70 Total Marks:100

ADVANCED POWER ELECTRONIC CONVERTERS
(Professional Elective III)

Course Code: GR20D5037 **L/T/P/C: 3/0/0/3**
I YEAR II SEMESTER

Course objectives

1. Explain the operation of advanced power electronic circuit topologies.
2. Summarize the control strategies involved in power electronic circuits.
3. How to analyze different DC-DC power supplies.
4. Analyze and design switched mode regulators for various industrial applications.
5. Propose few practical circuits, used in practice

Course outcomes

1. Valuate the design of APFC.
2. Analyze and design of Switched Mode power conversion topologies,
3. Analyze and design of DC-DC converters.
4. Analyze and design of resonant converters.
5. Design DC-DC convertors for different renewable energy sources

UNIT I BOOST TYPE APFC AND CONTROL

Introduction, Circuit Model Analysis, Design - Three phase utility interphases and control

UNIT II SMPS TOPOLOGIES

Buck regulators-condition for continuous inductor current and capacitor voltage, Boost regulators-condition for continuous inductor current and capacitor voltage, Buck-Boost regulators-condition for continuous inductor current and capacitor voltage. Cuk regulators-condition for continuous inductor current and capacitor voltage, Comparison of regulators.

UNIT III DC POWER SUPPLIES

DC power supplies-classification-switched mode dc power supplies-fly back Converter -forward converter- push pull converter-half bridge converter, Applications.

UNIT IV RESONANT CONVERTERS

Introduction, Class E resonant inverter, Zero Current Switching resonant converters-L type ZCS resonant converter-M type ZCS resonant converter-Zero Voltage Switching resonant converters-Two quadrant ZVS resonant converters, Resonant DC Link Inverters with Zero Voltage Switching.

UNIT V

Modelling and design of DC-DC Converters for various renewable energy – Small Signal Modelling, Conversion. Few power electronic circuits used in practice for controlling electric drives- Analysis and comparison of different PWM Techniques for Induction Motor drives.

Text Books

1. Rashid "Power Electronics" Prentice Hall India 2007.
2. G.K.Dubey et.al "Thyristorised Power Controllers" Wiley Eastern Ltd., 2005, 06.
3. Cyril W Lander "Power Electronics" McGraw Hill., 2005.
4. B. K Bose "Modern Power Electronics and AC Drives" Pearson Education (Asia)., 2007
5. Abraham Pressman "Switching Power Supply Design" McGraw Hill. 2001.

Timetable

I M.Tech. APEC – II Semester

Day/Hour	9-10	10-11	11-12	12-1	1-2	2-3	3-4
Monday	APEC			**BREAK**			
Tuesday							
Wednesday							
Thursday		APEC					
Friday							
Saturday							

Vision of the Institute

To be among the best of the institutions for engineers and technologists with attitudes, skills and knowledge and to become an epicenter of creative solutions.

Mission of the Institute

To achieve and impart quality education with an emphasis on practical skills and social relevance.

Vision of the Department

To impart technical knowledge and skills required to succeed in life, career and help society to achieve self sufficiency.

Mission of the Department

- To become an internationally leading department for higher learning.
- To build upon the culture and values of universal science and contemporary education.
- To be a center of research and education generating knowledge and technologies which lay groundwork in shaping the future in the fields of electrical and electronics engineering.
- To develop partnership with industrial, R&D and government agencies and actively participate in conferences, technical and community activities.

Program Educational Objectives (M.Tech. – EEE / Power Electronics)

Postgraduates will be able to

PEO 1: Have a successful technical or professional career, including supportive and leadership roles on multidisciplinary teams.

PEO 2: Acquire, use and develop skills as required for effective professional practices.

PEO 3: Able to attain holistic education that is an essential prerequisite for being a responsible member of society.

PEO 4: Engage in life-long learning, to remain abreast in their profession and be leaders in our technologically vibrant society.

Program Outcomes (M.Tech. – EEE / Power Electronics)

At the end of the Program, a post-graduate will have the ability to

PO 1: Apply knowledge of mathematics, science, and engineering.

PO 2: Design and conduct experiments, as well as to analyze and interpret data.

PO 3: Design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability.

PO 4: Function on multi-disciplinary teams.

PO 5: Identify, formulates, and solves engineering problems.

PO 6: Understanding of professional and ethical responsibility.

PO 7: Communicate effectively.

PO 8: Broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context.

PO 9: Recognition of the need for, and an ability to engage in life-long learning.

PO 10: Knowledge of contemporary issues.

PO 11: Utilize experimental, statistical and computational methods and tools necessary for engineering practice.

PO 12: Demonstrate an ability to design electrical and electronic circuits, power electronics, power systems; electrical machines analyze and interpret data and also an ability to design digital and analog systems and programming them.

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

COURSE OBJECTIVES

On completion of this Subject/Course the student shall be able to:

S.No	Objectives
1	Explain the operation of advanced power electronic circuit topologies
2	Summarize the control strategies involved in power electronic circuits
3	How to analyze different DC-DC power supplies
4	Analyze and design switched mode regulators for various industrial applications
5	Propose few practical circuits, used in practice

COURSE OUTCOMES

The expected outcomes of the Course/Subject are:

S.No	Outcomes
1.	Valuate the design of APFC
2.	Analyze and design of switched mode power conversion topologies.
3.	Analyze and design of DC-DC converters
4.	Analyze and design of resonant converters
5.	Design DC-DC converters for different renewable energy sources

Signature of faculty

Note: Please refer to Bloom's Taxonomy, to know the illustrative verbs that can be used to state the outcomes.

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Department of Electrical & Electronics Engineering

GUIDELINES TO STUDY THE COURSE / SUBJECT

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Guidelines to study the Course/ Subject: Advanced Power Electronic Converters

Course Design and Delivery System (CDD):

- The Course syllabus is written into number of learning objectives and outcomes.
- Every student will be given an assessment plan, criteria for assessment, scheme of evaluation and grading method.
- The Learning Process will be carried out through assessments of Knowledge, Skills and Attitude by various methods and the students will be given guidance to refer to the text books, reference books, journals, etc.

The faculty be able to –

- Understand the principles of Learning
- Understand the psychology of students
- Develop instructional objectives for a given topic
- Prepare course, unit and lesson plans
- Understand different methods of teaching and learning
- Use appropriate teaching and learning aids
- Plan and deliver lectures effectively
- Provide feedback to students using various methods of Assessments and tools of Evaluation
- Act as a guide, advisor, counselor, facilitator, motivator and not just as a teacher alone

Signature of HOD

Date:

Signature of faculty

Date:

Gokaraju Rangaraju Institute of Engineering and Technology
(Autonomous)

Department of Electrical & Electronics Engineering

COURSE SCHEDULE

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

The Schedule for the whole Course / Subject is:

S. No.	Description	Duration (Date)		Total No. Of Periods
		From	To	
1.	**UNIT-I:** Introduction of the Course & Unit-I Circuit Model Analysis, Boost type APFC Design - three phase utility, Interphases & control Problems	11.04.2022	25.04.2022	10
2.	**UNIT-II:** Buck Regulator Boost Regulator Buck-Boost Regulators Regulator Comparison of Regulator Derivation of Buck & Boost regulators Problems	28.04.2022	23.05.2022	14
3.	**UNIT-III:** DC Power Supplies introduction, switched mode DC power supplies classification & types Fly back converter Forward converter push pull converter half bridge converter	26.05.2022	16.06.2022	12
4.	**UNIT-IV:** Class E resonant inverter, ZCS resonant converter L-type ZCS resonant converter M-type ZCS resonant converter ZVS resonant converter Resonant DC link inverters Problems	20.06.2022	07.07.2022	12
5.	**UNIT-V:** Modelling & design of DC-DC converter small signal modelling Power electronics for controlling electric drives analysis & comparison of different PWM techniques for IM drives Problems Old question paper discussion	11.07.2022	04.08.2022	12

Total No. of Instructional periods available for the course: 60 Hours

ILLUSTRATIVE VERBS FOR STATING INSTRUCTIONAL OBJECTIVES

These verbs can also be used while framing questions for Continuous Assessment Examinations as well as for End – Semester (final)Examinations

ILLUSTRATIVE VERBS FOR STATING GENERAL OBJECTIVES/OUTCOMES

Know	**Understand**	**Design**

ILLUSTRATIVE VERBS FOR STATING SPECIFIC OBJECTIVES/OUTCOMES:

A. COGNITIVE DOMAIN (KNOWLEDGE)

1	2	3	4	5	6
Knowledge	**Comprehension Understanding**	**Application of knowledge & comprehension**	**Analysis Of whole w .r.t. its constituents**	**Synthesis**	**Evaluation Judgment**
Define	**Convert**	**Demonstrate**	**Differentiate**	**Categorize**	**Compare**
Identify	**Describe (a**	**Prepare**	**Discriminate**	**Combine**	
	Procedure)	**Relate**	**Distinguish**	**Design**	
	Distinguish	**Show**	**Separate**	**Generate**	
	Explain why/how	**Solve**		**Plan**	

B. AFFECTIVE DOMAIN (ATTITUDE)		C. PSYCHOMOTOR DOMAIN (SKILLS)				
Assist	**Select**	**Bend**	**Dissect**	**Insert**	**Perform**	**Straighten**
Change	**Develop**	**Calibrate**	**Draw**	**Keep**	**Prepare**	**Strengthen**
		Compress	**Extend**	**Elongate**	**Remove**	**Time**
		Conduct	**Feed**	**Limit**	**Replace**	**Transfer**
		Connect	**File**	**Manipulate**	**Report**	**Type**
		Convert	**Grow**	**Move Precisely**	**Reset**	**Weigh**
		Decrease	**Increase**	**Paint**	**Set**	

SCHEDULE OF INSTRUCTIONS
COURSE PLAN

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Unit No.	Lesson No.	Date	No. of Periods	Topics / Sub-Topics	Objectives & Outcomes Nos.	References (Textbook, Journal)
1.	1	11.04.2022	2	Introduction of the Course & Unit-I	1 1	Power Electronics MH Rashid
	2	14.04.2022	2	Circuit Model Analysis, Boost type APFC	1 1	Power Electronics MH Rashid
	3	18.04.2022	2	Design - three phase utility	1 1	Power Electronics MH Rashid
	4	21.04.2022	2	Interphases & control	1 1	Power Electronics MH Rashid
	5	25.04.2022	2	Problems	1 1	Power Electronics MH Rashid
2.	1	28.04.2022	2	Buck Regulator	2 2	Power Electronics MH Rashid
	2	02.05.2022	2	Boost Regulator	2 2	Power Electronics MH Rashid
	3	09.05.2022	2	Buck-Boost Regulator	2 2	Power Electronics MH Rashid
	4	12.05.2022	2	Cuk Regulator	2 2	Power Electronics MH Rashid
	5	16.05.2022	2	Comparison of Regulator	2 2	Power Electronics MH Rashid
	6	19.05.2022	2	Derivation of Buck & Boost regulators	2 2	Power Electronics MH Rashid
	7	23.05.2022	2	Problems	2 2	Power Electronics MH Rashid
3.	1	26.05.2022	2	DC Power Supplies introduction	3 3	Power Electronics MH Rashid
	2	30.05.2022	2	Switched mode DC power supplies classification & types	3 3	Power Electronics MH Rashid
	3	02.06.2022	2	Fly back converter	3 3	Power Electronics MH Rashid
	4	09.06.2022	2	Forward converter	3 3	Power Electronics MH Rashid
	5	13.06.2022	2	Push-pull converter	3 3	Power Electronics MH Rashid
	6	16.06.2022	2	Half bridge converter	3 3	Power Electronics MH Rashid

4	1	20.06.2022	2	Class E resonant inverter, ZCS resonant converter	4 4	Power Electronics MH Rashid
	2	23.06.2022	2	L type ZCS resonant converter	4 4	Power Electronics MH Rashid
	3	27.06.2022	2	M type ZCS resonant converter	4 4	Power Electronics MH Rashid
	4	30.06.2022	2	ZVS resonant converter	4 4	Power Electronics MH Rashid
	5	04.07.2022	2	Resonant DC link inverters	4 4	Power Electronics MH Rashid
	6	07.07.2022	2	Problems	4 4	Power Electronics MH Rashid
5	1	11.07.2022	2	Modelling & design of DC-DC converter	5 5	Power Electronics MH Rashid
	2	14.07.2022	2	small signal modelling	5 5	Power Electronics MH Rashid
	3	18.07.2022	2	Power electronics for controlling electric drives	5 5	Power Electronics MH Rashid
	4	21.07.2022	2	analysis & comparison of different PWM techniques for IM drives	5 5	Power Electronics MH Rashid
	5	25.07.2022	2	Problems	5 5	Power Electronics MH Rashid
	6	28.07.2022	2	Old question paper discussion	1,2,3,4,5 1,2,3,4,5	Power Electronics MH Rashid
	7	01.08.2022	2	Revision of unit-1&2	1 1	Power Electronics MH Rashid
	8	04.08.2022	2	Revision of unit-3&4	2 2	Power Electronics MH Rashid

Signature of HOD

Signature of faculty

Date:

Date:

Note: 1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED IN BOLD
3. MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC.

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SCHEDULE OF INSTRUCTIONS
UNIT - I PLAN

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No.	Date	No. of Periods	Topics / Sub-Topics	Objectives & Outcomes Nos.	References (Textbook, Journal)
1	11.04.2022	2	Introduction of the Course & Unit-I	1 1	Power Electronics MH Rashid
2	14.04.2022	2	Circuit Model Analysis, Boost type APFC	1 1	Power Electronics MH Rashid
3	18.04.2022	2	Design - three phase utility	1 1	Power Electronics MH Rashid
4	21.04.2022	2	Interphases & control	1 1	Power Electronics MH Rashid
5	25.04.2022	2	Problems	1 1	Power Electronics MH Rashid

Signature of HOD

Date:

Signature of faculty

Date:

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Department of Electrical & Electronics Engineering

SCHEDULE OF INSTRUCTIONS

UNIT - II PLAN

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No.	Date	No. of Periods	Topics / Sub-Topics	Objectives & Outcomes Nos.	References (Textbook, Journal)
1	28.04.2022	2	Buck Regulator	2 2	Power Electronics MH Rashid
2	02.05.2022	2	Boost Regulator	2 2	Power Electronics MH Rashid
3	09.05.2022	2	Buck-Boost Regulator	2 2	Power Electronics MH Rashid
4	12.05.2022	2	Cuk Regulator	2 2	Power Electronics MH Rashid
5	16.05.2022	2	Comparison of Regulator	2 2	Power Electronics MH Rashid
6	19.05.2022	2	Derivation of Buck & Boost regulators	2 2	Power Electronics MH Rashid
7	23.05.2022	2	Problems	2 2	Power Electronics MH Rashid

Signature of HOD

Signature of faculty

Date:

Date:

Note: 1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED IN BOLD
3. MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC.

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Department of Electrical & Electronics Engineering

SCHEDULE OF INSTRUCTIONS

UNIT - III PLAN

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No.	Date	No. of Periods	Topics / Sub-Topics	Objectives & Outcomes Nos.	References (Textbook, Journal)
1	26.05.2022	2	DC Power Supplies introduction	3 3	Power Electronics MH Rashid
2	30.05.2022	2	Switched mode DC power supplies classification & types	3 3	Power Electronics MH Rashid
3	02.06.2022	2	Fly back converter	3 3	Power Electronics MH Rashid
4	09.06.2022	2	Forward converter	3 3	Power Electronics MH Rashid
5	13.06.2022	2	Push-pull converter	3 3	Power Electronics MH Rashid
6	16.06.2022	2	Half bridge converter	3 3	Power Electronics MH Rashid

Signature of HOD

Signature of faculty

Date:

Date:

Note: 1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED IN BOLD
3. MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC.

SCHEDULE OF INSTRUCTIONS

UNIT - IV PLAN

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No.	Date	No. of Periods	Topics / Sub-Topics	Objectives & Outcomes Nos.	References (Textbook, Journal)
1	20.06.2022	2	Class E resonant inverter, ZCS resonant converter	4 4	Power Electronics MH Rashid
2	23.06.2022	2	L type ZCS resonant converter	4 4	Power Electronics MH Rashid
3	27.06.2022	2	M type ZCS resonant converter	4 4	Power Electronics MH Rashid
4	30.06.2022	2	ZVS resonant converter	4 4	Power Electronics MH Rashid
5	04.07.2022	2	Resonant DC link inverters	4 4	Power Electronics MH Rashid
6	07.07.2022	2	Problems	4 4	Power Electronics MH Rashid

Signature of HOD

Date:

Signature of faculty

Date:

Note: 1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED IN BOLD
3. MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC.

SCHEDULE OF INSTRUCTIONS

UNIT -V PLAN

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No.	Date	No. of Periods	Topics / Sub-Topics	Objectives & Outcomes Nos.	References (Textbook, Journal)
1	11.07.2022	2	Modelling & design of DC-DC converter	5 5	Power Electronics MH Rashid
2	14.07.2022	2	small signal modelling	5 5	Power Electronics MH Rashid
3	18.07.2022	2	Power electronics for controlling electric drives	5 5	Power Electronics MH Rashid
4	21.07.2022	2	analysis & comparison of different PWM techniques for IM drives	5 5	Power Electronics MH Rashid
5	25.07.2022	2	Problems	5 5	Power Electronics MH Rashid
6	28.07.2022	2	Old question paper discussion	1,2,3,4,5 1,2,3,4,5	Power Electronics MH Rashid
7	01.08.2022	2	Revision of unit-1&2	1 1	Power Electronics MH Rashid
8	04.08.2022	2	Revision of unit-3&4	2 2	Power Electronics MH Rashid

Signature of HOD

Date:

Signature of faculty

Date:

Note: 1. ENSURE THAT ALL TOPICS SPECIFIED IN THE COURSE ARE MENTIONED.
2. ADDITIONAL TOPICS COVERED, IF ANY, MAY ALSO BE SPECIFIED IN BOLD
3. MENTION THE CORRESPONDING COURSE OBJECTIVE AND OUT COME NUMBERS AGAINST EACH TOPIC.

LESSON PLAN (U-I)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 01 Duration of Lesson: 1hr30 MIN

Lesson Title: Introduction of the Course & Unit-I

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand three phase utilities usage in day life.
To familiarize students on Boost type APFC
To understand students the concept of Interphases & control and their need for its improvement.
To provide information on global scenario of APFC.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
70 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment – I & tutorial-I sheets

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-I)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 02 Duration of Lesson: 1hr30 MIN

Lesson Title: Circuit Model Analysis, Boost type APFC

INSTRUCTIONAL/LESSON OBJECTIVES:
To make students understand three phase utilities usage in day life.
To familiarize students on Boost type APFC
To understand students the concept of Interphases & control and their need for its improvement.
To provide information on global scenario of APFC.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions: .
Refer assignment – I & tutorial-I sheets

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos..1,2,3,4 & 1,3.

LESSON PLAN (U-I)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 03 Duration of Lesson: 1hr30 MIN

Lesson Title: Design - three phase utility

INSTRUCTIONAL/LESSON OBJECTIVES:
To make students understand three phase utilities usage in day life.
To familiarize students on Boost type APFC
To understand students the concept of Interphases & control and their need for its improvement.
To provide information on global scenario of APFC.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions: .

Refer assignment – I & tutorial-I sheets

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos..1,2,3,4 & 1,3.

LESSON PLAN (U-I)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 04 Duration of Lesson: 1hr30 MIN

Lesson Title: Interphases & control

INSTRUCTIONAL/LESSON OBJECTIVES:
To make students understand three phase utilities usage in day life.
To familiarize students on Boost type APFC
To understand students the concept of Interphases & control and their need for its improvement.
To provide information on global scenario of APFC.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions:
Refer assignment – I & tutorial-I sheets

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos..1,2,3,4 & 1,3.

LESSON PLAN (U-I)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 05 Duration of Lesson: 1hr30 MIN

Lesson Title: Problems

INSTRUCTIONAL/LESSON OBJECTIVES:
To make students understand three phase utilities usage in day life.
To familiarize students on Boost type APFC
To understand students the concept of Interphases & control and their need for its improvement.
To provide information on global scenario of APFC.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions: .
Refer assignment – I & tutorial-I sheets

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos..1,2,3,4 & 1,3.

LESSON PLAN (U-II)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 01 Duration of Lesson: 1hr30 MIN

Lesson Title: Buck Regulator

INSTRUCTIONAL/LESSON OBJECTIVES:
To make students understand the concept of regulators & their need in day life.
To familiarize students on Buck and Boost type regulators
To understand students the concept of Cuk Regulator.
To provide information on global scenario of Buck-Boost regulators

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
70 min for the class
15 min for doubts

Assignment / Questions: .
Refer assignment-II & tutorial-II sheets

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos..1,2,3,4 & 1,3.

LESSON PLAN (U-II)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 02 Duration of Lesson: 1hr30 MIN

Lesson Title: Boost Regulator

INSTRUCTIONAL/LESSON OBJECTIVES:
To make students understand the concept of regulators & their need in day life.
To familiarize students on Buck and Boost type regulators
To understand students the concept of Cuk Regulator.
To provide information on global scenario of Buck-Boost regulators.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions: .
Refer assignment-II & tutorial-II sheets

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos..1,2,3,4 & 1,3.

LESSON PLAN (U-II)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 03 Duration of Lesson: 1hr30 MIN

Lesson Title: Buck-Boost Regulator

INSTRUCTIONAL/LESSON OBJECTIVES:
To make students understand the concept of regulators & their need in day life.
To familiarize students on Buck and Boost type regulators
To understand students the concept of Cuk Regulator.
To provide information on global scenario of Buck-Boost regulators.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment-II & tutorial-II sheets.

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-II)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 04 Duration of Lesson: 1hr30 MIN

Lesson Title: Cuk Regulator

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of regulators & their need in day life.
To familiarize students on Buck and Boost type regulators
To understand students the concept of Cuk Regulator.
To provide information on global scenario of Buck-Boost regulators.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment-II & tutorial-II sheets

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-II)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 05 Duration of Lesson: 1hr30 MIN

Lesson Title: Comparison of Regulator

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of regulators & their need in day life.
To familiarize students on Buck and Boost type regulators
To understand students the concept of Cuk Regulator.
To provide information on global scenario of Buck-Boost regulators.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment-II & tutorial-II sheets.

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-II)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 06 Duration of Lesson: 1hr30 MIN

Lesson Title: Derivation of Buck & Boost regulators

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of regulators & their need in day life.
To familiarize students on Buck and Boost type regulators
To understand students the concept of Cuk Regulator.
To provide information on global scenario of Buck-Boost regulators.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment-II & tutorial-II sheets

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-II)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 07 Duration of Lesson: 1hr30 MIN

Lesson Title: Problems

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of regulators & their need in day life.
To familiarize students on Buck and Boost type regulators
To understand students the concept of Cuk Regulator.
To provide information on global scenario of Buck-Boost regulators.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment-II & tutorial-II sheets.

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-III)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 01 Duration of Lesson: 1hr30 MIN

Lesson Title: DC Power Supplies introduction

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of DC Power Supplies.
To familiarize students on Fly back & Forward converter.
To understand the concept of Switched mode DC power supplies classification & types.
To provide information on push-pull and half bridge converter.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance 70 min for the class 15 min for doubts

Assignment / Questions:

Refer assignment-III & tutorial-III sheets

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-III)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 02 Duration of Lesson: 1hr30 MIN

Lesson Title: Switched mode DC power supplies classification & types

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of DC Power Supplies.
To familiarize students on Fly back & Forward converter.
To understand the concept of Switched mode DC power supplies classification & types.
To provide information on push-pull and half bridge converter.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment-III & tutorial-III sheets

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-III)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 03 Duration of Lesson: 1hr30 MIN

Lesson Title: Fly back converter

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of DC Power Supplies.
To familiarize students on Fly back & Forward converter.
To understand the concept of Switched mode DC power supplies classification & types.
To provide information on push-pull and half bridge converter.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment-III & tutorial-III sheets

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-III)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 04 Duration of Lesson: 1hr30 MIN

Lesson Title: Forward converter

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of DC Power Supplies.
To familiarize students on Fly back & Forward converter.
To understand the concept of Switched mode DC power supplies classification & types.
To provide information on push-pull and half bridge converter.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment-III & tutorial-III sheets

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-III)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 05 Duration of Lesson: 1hr30 MIN

Lesson Title: Push-pull converter

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of DC Power Supplies.
To familiarize students on Fly back & Forward converter.
To understand the concept of Switched mode DC power supplies classification & types.
To provide information on push-pull and half bridge converter.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment-III & tutorial-III sheets

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-III)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 06 Duration of Lesson: 1hr30 MIN

Lesson Title: Half bridge converter

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of DC Power Supplies.
To familiarize students on Fly back & Forward converter.
To understand the concept of Switched mode DC power supplies classification & types.
To provide information on push-pull and half bridge converter.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment-III & tutorial-III sheets

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-IV)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 01 Duration of Lesson: 1hr30 MIN

Lesson Title: Class E resonant inverter, ZCS resonant converter

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of Class E resonant inverter, ZCS resonant converter.
To familiarize students on L & M type ZCS resonant converters.
To understand the concept of ZVS resonant converter.
To provide information on Resonant DC link inverters

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
70 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment-IV & tutorial-IV sheets.

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-IV)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 02 Duration of Lesson: 1hr30 MIN

Lesson Title: L type ZCS resonant converter

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of Class E resonant inverter, ZCS resonant converter.
To familiarize students on L & M type ZCS resonant converters.
To understand the concept of ZVS resonant converter.
To provide information on Resonant DC link inverters.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment-IV & tutorial-IV sheets.

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-IV)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 03 Duration of Lesson: 1hr30 MIN

Lesson Title: M type ZCS resonant converter

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of Class E resonant inverter, ZCS resonant converter.
To familiarize students on L & M type ZCS resonant converters.
To understand the concept of ZVS resonant converter.
To provide information on Resonant DC link inverters.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment-IV & tutorial-IV sheets

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-IV)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 04 Duration of Lesson: 1hr30 MIN

Lesson Title: ZVS resonant converter

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of Class E resonant inverter, ZCS resonant converter.
To familiarize students on L & M type ZCS resonant converters.
To understand the concept of ZVS resonant converter.
To provide information on Resonant DC link inverters.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment-IV & tutorial-IV sheets.

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-IV)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 05 Duration of Lesson: 1hr30 MIN

Lesson Title: Resonant DC link inverters

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of Class E resonant inverter, ZCS resonant converter.
To familiarize students on L & M type ZCS resonant converters.
To understand the concept of ZVS resonant converter.
To provide information on Resonant DC link inverters.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment-IV & tutorial-IV sheets.

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-IV)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 06 Duration of Lesson: 1hr30 MIN

Lesson Title: Problems

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of Class E resonant inverter, ZCS resonant converter.
To familiarize students on L & M type ZCS resonant converters.
To understand the concept of ZVS resonant converter.
To provide information on Resonant DC link inverters.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment-IV & tutorial-IV sheets.

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-V)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 01 Duration of Lesson: 1hr30 MIN

Lesson Title: Modelling & design of DC-DC converter

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of Modelling & design of DC-DC converter.
To familiarize students on Power electronics for controlling electric drives.
To understand the concept of small signal modelling.
To provide information on analysis & comparison of different PWM techniques for IM drives.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance 70 min for the class 15 min for doubts

Assignment / Questions:

Refer assignment-V & tutorial-V sheets

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-V)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 02 Duration of Lesson: 1hr30 MIN

Lesson Title: small signal modelling

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of Modelling & design of DC-DC converter.
To familiarize students on Power electronics for controlling electric drives.
To understand the concept of small signal modelling.
To provide information on analysis & comparison of different PWM techniques for IM drives.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment-V & tutorial-V sheets

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-V)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 03 Duration of Lesson: 1hr30 MIN

Lesson Title: Power electronics for controlling electric drives

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of Modelling & design of DC-DC converter.
To familiarize students on Power electronics for controlling electric drives.
To understand the concept of small signal modelling.
To provide information on analysis & comparison of different PWM techniques for IM drives.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment-V & tutorial-V sheets.

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-V)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 04 Duration of Lesson: 1hr30 MIN

Lesson Title: analysis & comparison of different PWM techniques for IM drives

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of Modelling & design of DC-DC converter.
To familiarize students on Power electronics for controlling electric drives.
To understand the concept of small signal modelling.
To provide information on analysis & comparison of different PWM techniques for IM drives.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment-V & tutorial-V sheets.

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

LESSON PLAN (U-V)

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Lesson No: 05 Duration of Lesson: 1hr30 MIN

Lesson Title: Problems

INSTRUCTIONAL/LESSON OBJECTIVES:

To make students understand the concept of Modelling & design of DC-DC converter.
To familiarize students on Power electronics for controlling electric drives.
To understand the concept of small signal modelling.
To provide information on analysis & comparison of different PWM techniques for IM drives.

TEACHING AIDS :PPTs
TEACHING POINTS :

5 mins for taking attendance
15 for revision of previous class
55 min for the class
15 min for doubts

Assignment / Questions:

Refer assignment-V & tutorial-V sheets

Signature of faculty

Note: Mention for each question the relevant Objectives and Outcomes Nos.1,2,3,4 & 1,3..

ASSIGNMENT SHEET – 1

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

This Assignment corresponds to Unit No. 1

Q1. In detail discuss three phase utility interphases

Q2. Discuss circuit model of boost type APFC

Q3 Define utility interface

Please write the Questions / Problems / Exercises which you would like to give to the students and mention the Objectives/Outcomes to which these Questions / Problems / Exercises are related.

Objective Nos.: 1

Outcome Nos.: 1

Signature of HOD

Date:

Signature of faculty

Date:

ASSIGNMENT SHEET – 2

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

This Assignment corresponds to Unit No. 2

Q1. Derive the condition for continuous inductor current of a Boost Regulator.

Q2. Discuss Buck-Boost regulator for the condition of continuous capacitor voltage.

Q3. What is Boost Regulator. Derive the condition for continuous inductor current

Please write the Questions / Problems / Exercises which you would like to give to the students and also mention the Objectives/Outcomes to which these Questions / Problems / Exercises are related.

Objective Nos.: 2

Outcome Nos.: 2

Signature of HOD

Date:

Signature of faculty

Date:

ASSIGNMENT SHEET – 3

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

This Assignment corresponds to Unit No. 3

Q1. Discuss forward converter with necessary circuit diagrams and output waveforms.

Q2. Discuss half bridge converter with necessary circuit diagrams and output waveforms

Q3. Explain fly back converter with circuit diagram & waveforms

Please write the Questions / Problems / Exercises which you would like to give to the students and also mention the Objectives/Outcomes to which these Questions / Problems / Exercises are related.

Objective Nos.: 3

Outcome Nos.: 3

Signature of HOD

Date:

Signature of faculty

Date:

ASSIGNMENT SHEET – 4

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

This Assignment corresponds to Unit No. 4

Q1. Discuss M-type ZCS based resonant converter with circuit diagram & necessary waveforms.

Q2. Discuss two quadrant ZVS resonant converter with circuit diagram & necessary waveforms.

Q3. Discuss Class-E resonant rectifier

Please write the Questions / Problems / Exercises which you would like to give to the students and also mention the Objectives/Outcomes to which these Questions / Problems / Exercises are related.

Objective Nos.: 4

Outcome Nos.: 4

Signature of HOD

Date:

Signature of faculty

Date:

ASSIGNMENT SHEET – 5

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

This tutorial corresponds to Unit No. 5

Q1. Compare different PWM techniques used for Induction Motor Drive

Q2. Discuss DC-DC converter used in renewable energy interface with appropriate circuit diagram & waveform

Q3. Explain two quadrant ZVS resonant converter

Please write the Questions / Problems / Exercises which you would like to give to the students and also mention the Objectives/Outcomes to which these Questions / Problems / Exercises are related.

Objective Nos.: 5

Outcome Nos.: 5

Signature of HOD

Date:

Signature of faculty

Date:

TUTORIAL SHEET – 1

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

This tutorial corresponds to Unit No. 1

Q1. What is APFC

Q2. DC Converters can be used as switching-mode regulators to convert a DC voltage, normally _____ to a _____ DC output voltage.
a. Unregulated, Regulated b. Regulated, Unregulated
c. Fixed, Variable d. Variable, Fixed

Q3. Ripple Content is normally reduced by an _____ filter.
a. LC b. L c. C d. All the above.

Q4. Define utility interface.

Please write the Questions / Problems / Exercises which you would like to give to the students and also mention the Objectives/Outcomes to which these Questions / Problems / Exercises are related.

Objective Nos.: 1

Outcome Nos.: 1

Signature of HOD Signature of faculty

Date: Date:

TUTORIAL SHEET – 2

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

This tutorial corresponds to Unit No. 2

Q1. In buck regulator, the average output voltage is _____ the input voltage
a. Less than b. Greater than c. Equal d. none.

Q2. The critical value of the inductor Lc in boost regulator is _____.
a. k(1-k)R/2f b. k(1+k)R/2f c. (1-k)R/2f d. (1+k)R/2f.

Q3. A boost regulator can _____ the output voltage without transformer
a. Step-up b. Step-down c. Isolate d. None

Please write the Questions / Problems / Exercises which you would like to give to the students and also mention the Objectives/Outcomes to which these Questions / Problems / Exercises are related.

Objective Nos.: 2

Outcome Nos.: 2

Signature of HOD

Date:

Signature of faculty

Date:

TUTORIAL SHEET – 3

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

This tutorial corresponds to Unit No. 3

Q1. The switching mode supplies have high efficiency and can supply a ____ load current at _____ voltage

a. high, low b. low, high c. high, high d. low, low

Q2 Fly back converter generally operates _____ mode of operation

a. Discontinuous b. Continuous c. Isolate d. None

Q3. Flyback converter is used mostly in applications below _____

a. 100kW b. 200kW c. 300kW d. 400kW

Q4. Forward converter is similar to _____ converter

a. flyback b. push-pull
c. half-bridge d. full-bridge.

Please write the Questions / Problems / Exercises which you would like to give to the students and also mention the Objectives/Outcomes to which these Questions / Problems / Exercises are related.

Objective Nos.: 3

Outcome Nos.: 3

Signature of HOD Signature of faculty

Date: Date:

Gokaraju Rangaraju Institute of Engineering and Technology
(Autonomous)

Department of Electrical & Electronics Engineering

TUTORIAL SHEET – 4

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

This tutorial corresponds to Unit No. 4

Q1. In DC power supply the common practice is to use_____ stage conversion
a. Two b. Three
c. One d. Four

Q2. The DC-AC conversion can be accomplished by _____.
a. PWM b. Single Pulse c. Multiple Pulse d. All the above

Q3. Switching mode supplies have high efficiency and can supply _____ load current at _____ voltage
a. High, Low b. Low, Low c. Low, High d. High, High

Q4. Fly back converter, mainly operates in _____mode of operation
a. Discontinuous b. Continuous c. Stability d. none

Q5. The push-pull converter is often driven by a constant current source such that primary current is a _____ wave
a. square b. Triangular c. saw tooth d. trapezoidal?

Please write the Questions / Problems / Exercises which you would like to give to the students and also mention the Objectives/Outcomes to which these Questions / Problems / Exercises are related.

Objective Nos.: 4

Outcome Nos.: 4

Signature of HOD Signature of faculty

Date: Date:

TUTORIAL SHEET – 5

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

This tutorial corresponds to Unit No. 5

Q1. Forward converter is widely used with output power below _____ W
a. 1000 b. 200 c. 500 d. 700

Q2. The switches of a ZCS resonant convert turn on and off at _____
a. peak current b. zero current c. rms current d. zero voltage

Q3. Class E resonant inverter uses only one transistor has an efficiency of _____
a. 97% b. 95% c. 96% d. 98%

Q4. The switches of a ZVS resonant convert turn on and off at _____
a. peak current b. zero voltage c. rms current d. zero current

Q5. Capacitor is connected in parallel with the switch to achieve _____
a. ZCS b. ZVS
c. Class-E d. full-bridge

Please write the Questions / Problems / Exercises which you would like to give to the students and also mention the Objectives/Outcomes to which these Questions / Problems / Exercises are related.

Objective Nos.: 5

Outcome Nos.: 5

Signature of HOD Signature of faculty

Date: Date:

EVALUATION STRATEGY

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Target

a. Percentage of Pass : 95%

Method of Evaluation

a. Daily Attendance
b. Assignments
c. Online Quiz & Seminars
d. Internal Examinations
e. Semester / End Examination

List out any new topic(s) or any innovation you would like to introduce in teaching the subjects in this semester

Case Study of any one existing application

Signature of HOD

Date:

Signature of faculty

Date:

Gokaraju Rangaraju Institute of Engineering and Technology
(Autonomous)

Department of Electrical & Electronics Engineering

COURSE COMPLETION STATUS

Academic Year	: 2021-22	Semester	: II
Name of the Program	: I M.Tech - EEE (PE)		
Course	: Advanced Power Electronic Converters	Course Code	: GR20D5037
Name of the Faculty	: Dr. Suresh Kumar Tummala, Professor	Department	: EEE

Actual Date of Completion & Remarks if any

Units	Remarks	No. of Objectives Achieved	No. of Outcomes Achieved
Unit 1	completed on 31.05.2021	1	1
Unit 2	completed on 23.06.2021	2	2
Unit 3	completed on 11.08.2021	3	3
Unit 4	completed on 01.09.2021	4	4
Unit 5	completed on 06.10.2021	5	5

Signature of HOD

Date:

Signature of faculty

Date:

Note: After the completion of each unit mention the number of Objectives & Outcomes Achieved.

Name of the Course: Advanced Power Electronic Converter

Assessment methods:

1. Regular Attendance to Classes.
2. Mid Exam / Main Exam.
3. Written class tests clearly linked to learning objectives / Quiz through Moodle
4. Classroom assessment techniques via. Tutorials and assignments.
5. Seminars.

1. Program Educational Objectives (PEOs) – Vision/Mission Matrix

(Indicate the relationships by mark "X")

Vision / Mission / PEOs	Vision of the Institute	Mission of the Institute	Mission of the Program
1	X		X
2	X	X	X
3	X	X	X
4		X	X

2. Program Educational Objectives(PEOs)-Program Outcomes(POs) Relationship Matrix

(Indicate the relationships by mark "X")

P-Outcomes / PEOs	a	b	c	d	e	f	g	h	i	j	k	l
1	X	X	X	X	X			X	X	X	X	X
2	X	X	X	X	X			X	X	X	X	X
3		X	X	X		X	X	X	X	X		
4				X					X	X		X

3. Course Objectives-Course Outcomes Relationship Matrix

(Indicate the relationships by mark "X")

Course-Outcomes / Course-Objectives	1	2	3	4	5
1	X		X		
2		X		X	
3			X		X
4	X		X		
5	X		X		

4. Course Objectives-Program Outcomes (POs) Relationship Matrix

(Indicate the relationships by mark "X")

P-Outcomes / C-Objectives	a	b	c	d	e	f	g	h	i	j	k	l
1	X		X		X	X	X	X	X	X	X	
2	X	X	X		X	X	X	X			X	X
3	X	X	X		X	X	X	X	X		X	X
4	X	X		X	X		X	X		X	X	X
5	X	X		X	X		X	X		X	X	X

5. Course Outcomes-Program Outcomes (POs) Relationship Matrix

(Indicate the relationships by mark "X")

P-Outcomes / C-Outcomes	a	b	c	d	e	f	g	h	i	j	k	l
1	X				X	X	X	X	X		X	X
2	X	X	X	X	X		X	X	X		X	X
3	X	X		X	X		X	X	X	X	X	X
4		X	X				X			X		X
5			X		X		X		X			

6. Courses (with title & code)-Program Outcomes (POs) Relationship Matrix
(Indicate the relationships by mark "X")

P-Outcomes / Courses	a	b	c	d	e	f	g	h	i	j	k	l
APEC (GR20D5037)	X	X	X		X	X	X	X		X	X	X

7. Program Educational Objectives (PEOs)-Course Outcomes Relationship Matrix
(Indicate the relationships by mark "X")

P-Objectives (PEOs) / Course-Outcomes	1	2	3	4
1		X	X	X
2	X	X	X	X
3	X	X	X	X
4		X	X	X
5		X	X	X

8. Assignments & Assessments-Program Outcomes (POs) Relationship Matrix
(Indicate the relationships by mark "X")

P-Outcomes / Assessments	a	b	c	d	e	f	g	h	i	j	k	l
1	X			X	X	X	X	X	X	X		
2	X	X			X		X	X	X	X		
3	X				X	X			X			
4	X			X	X	X		X	X	X		X
5	X	X		X			X		X		X	

9. Assignments & Assessments-Program Educational Objectives (PEOs) Relationship Matrix (Indicate the relationships by mark "X")

P-Objectives (PEOs) / Assessments	1	2	3	4
1		X	X	X
2	X	X	X	X
3	X	X		X
4		X		X
5	X	X	X	X

Rubric

Performance Criteria	Unsatisfactory	Developing	Satisfactory	Exemplary
	1	**2**	**3**	**4**
Research & Gather Information	Does not collect any information that relates to the topic	Collects very little information some relates to the topic	Collects some basic Information most relates to the topic	Collects a great deal of Information all relates to the topic
Fulfill team role's duty	Does not perform any duties of assigned team role.	Performs very little duties.	Performs nearly all duties.	Performs all duties of assigned team role.
Share Equally	Always relies on others to do the work.	Rarely does the assigned work - often needs reminding.	Usually does the assigned work - rarely needs reminding.	Always does the assigned work without having to be reminded
Listen to other team mates	Is always talking—never allows anyone else to speak.	Usually doing most of the talking-- rarely allows others to speak.	Listens, but sometimes talks too much.	Listens and speaks a fair amount.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
(Autonomous)
Department of EEE

I-M. Tech (Power Electronics) II-Sem **I-Mid** **Marks: 5M**

Time: 15 Minutes **Date of Exam: 08-06-2022**

Subject: **Advanced Power Electronic Converters (GR20D5037)**

Name: **Roll Number:**

Note: Answer all questions. All questions carry equal marks. **Total: 5M**

1.	DC Converters can be used as switching-mode regulators to convert a DC voltage, normally _____ to a _____ DC output voltage. a. Unregulated, Regulated b. Regulated, Unregulated c. Fixed, Variable d. Variable, Fixed	[a]	BL 1	CO 1
2.	Ripple Content is normally reduced by an _____ filter. a. LC b. L c. C d. All the above	[a]	BL 2	CO 1
3.	If a transistor has a switching time of 0.5μs, the oscillator period would be 50μs, which gives the maximum oscillator frequency of _____ a. 20kHz b. 10kHz c. 5kHz d. 25kHz	[a]	BL 3	CO 1
4.	In buck regulator, the average output voltage is _____ the input voltage a. Less than b. Greater than c. Equal d. none	[a]	BL 3	CO 2
5.	The critical value of the inductor L_c in boost regulator is _____. a. k(1-k)R/2f b. k(1+k)R/2f c. (1-k)R/2f d. (1+k)R/2f	[a]	BL 4	CO 2
6.	A boost regulator can _____ the output voltage without transformer a. Step-up b. Step-down c. Isolate d. None	[b]	BL 2	CO 2
7.	The switching mode supplies have high efficiency and can supply a ____ load current at _____ voltage a. high, low b. low, high c. high, high d. low, low	[b]	BL 5	CO 2
8.	Fly back converter generally operates _____ mode of operation a. Discontinuous b. Continuous c. Isolate d. None	[b]	BL 3	CO 3
9.	Flyback converter is used mostly in applications below _____ a. 100kW b. 200kW c. 300kW d. 400kW	[b]	BL 5	CO 3
10.	Forward converter is similar to _____ converter a. flyback b. push-pull c. half-bridge d. full-bridge	[b]	BL 6	CO 3

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
(Autonomous)
Department of EEE

I-M. Tech (Power Electronics) II-Sem **I-Mid** **Marks: 15M**

Time: 75 Minutes **Date of Exam: 08-06-2022**

Subject: **Advanced Power Electronic Converters (GR20D5037)**

Note: Answer all questions. All questions carry equal marks. **Total: 3 x 5 = 15M**

1.A	Discuss Three-Phase Utility Interphases	BL 3&4	CO 1
	OR		
1.B	Explain Boost type APFC with circuit diagram & necessary waveforms	BL 2&3	CO 1
2.A	What is Boost Regulator. Derive the condition for continuous inductor current	BL 3&4	CO 2
	OR		
2.B	Discuss Buck-Boost regulator for the condition of continuous capacitor voltage	BL 3&4	CO 2
3.A	Explain fly back converter with circuit diagram & waveforms	BL 3&4	CO 3
	OR		
3.B	Derive the efficiency expression of flyback converter	BL 5&6	CO 3

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
(Autonomous)
Department of EEE

M. Tech (Power Electronics) II-Sem **II-Mid** **Marks: 5M**

Time: 15 Minutes **Date of Exam: 17-08-2022**

Subject: **Advanced Power Electronic Converters (GR20D5037)**

Name: **Roll Number:**

Note: Answer all questions. All questions carry equal marks. **Total: 5M**

1.	In DC power supply the common practice is to use_____ stage conversion a. Two b. Three c. One d. Four	[a]	CO-3	BL 1
2.	The DC-AC conversion can be accomplished by _____. a. PWM b. Single Pulse c. Multiple Pulse d. All the above	[a]	CO-3	BL 2
3.	Switching mode supplies have high efficiency and can supply _____ load current at _____ voltage a. High, Low b. Low, Low c. Low, High d. High, High	[a]	CO-3	BL 3
4.	Fly back converter, mainly operates in _____mode of operation a. Discontinuous b. Continuous c. Stability d. none	[a]	CO-4	BL 3
5.	The push-pull converter is often driven by a constant current source such that primary current is a _____ wave a. square b. Triangular c. saw tooth d. trapezoidal	[a]	CO-4	BL 4
6.	Forward converter is widely used with output power below _____ W a. 1000 b. 200 c. 500 d. 700	[b]	CO-4	BL 2
7.	The switches of a ZCS resonant convert turn on and off at _____ a. peak current b. zero current c. rms current d. zero voltage	[b]	CO-5	BL 5
8.	Class E resonant inverter uses only one transistor has an efficiency of a. 97% b. 95% c. 96% d. 98%	[b]	CO-5	BL 3
9.	The switches of a ZVS resonant convert turn on and off at _____ a. peak current b. zero voltage c. rms current d. zero current	[b]	CO-5	BL 5
10.	Capacitor is connected in parallel with the switch to achieve _____ a. ZCS b. ZVS c. Class-E d. full-bridge	[b]	CO-5	BL 6

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
(Autonomous)
Department of EEE

M. Tech (Power Electronics) II-Sem **II-Mid** **Marks: 15M**

Time: 75 Minutes **Date of Exam: 17-08-2022**

Subject: **Advanced Power Electronic Converters (GR20D5037)**

Note: Answer all questions. All questions carry equal marks. **Total: 3 x 5 = 15M**

1.A	With appropriate circuit discuss forward converter	CO-3	BL 3&4
	OR		
1.B	Explain the four modes of operation of Half-bridge converter	CO-3	BL 2&3
2.A	With appropriate circuit discuss flyback converter	CO-3	BL 3&4
	OR		
2.B	Discuss Class-E resonant rectifier	CO-4	BL 3&4
3.A	Explain L-type ZCS resonant converter with circuit diagram & waveforms	CO-4	BL 3&4
	OR		
3.B	Explain two quadrant ZVS resonant converter	CO-5	BL 5&6

2021-22 M.Tech Power Electronics - Advanced Power Electronic Converters

S.No	Roll No	Name	Mid-I		
			Obj (5M)	Des (15M)	Total (20M)
1	21241D4301	Pujitha Dupati	1.50	8.00	10
2	21241D4302	Kothapalli Malini	1.50	9.00	11
3	21241D4303	Moshina Begum	3.50	11.00	15
4	21241D4304	Surya Prakash Yadav	2.50	13.00	16

2021-22 M.Tech Power Electronics - Advanced Power Electronic Converters

S.No	Roll No	Name	Mid-II		
			Obj (5M)	Des (15M)	Total (20M)
1	21241D4301	Pujitha Dupati	0.5	7.00	8
2	21241D4302	Kothapalli Malini	0	10.00	10
3	21241D4303	Moshina Begum	3	12.00	15
4	21241D4304	Surya Prakash Yadav	2	13.00	15

A High Power-Quality, Three-Phase Utility Interface

Bunyamin Tamyurek and David A. Torrey
Department of Electric Power Engineering
Rensselaer Polytechnic Institute
110 8th Street
Troy, NY 12180-3590

Abstract: **This paper presents a new three-phase ac/dc converter topology that provides a high-power-factor interface to the utility. The circuit topology of the converter is based on the discontinuous mode flyback converter. The objective of this work is to develop the technology for the proposed converter to meet the high-power factor requirements and to serve the demand for an advanced high-power, inexpensive, efficient and small size ac/dc rectifier in the telecommunications market. A laboratory proof-of-concept converter intended for 12.5 kW output was built to investigate the performance of the proposed converter in a practical application. The experimental results verify that the proposed converter achieves a near-unity power factor at the input and a constant voltage at the load side of the interface. However, the efficiency of the converter measured lower than expected. Further study revealed that the low efficiency is due to the adverse effects of the parasitic inductances on the energy transfer to the output. The effects of the parasitics on the converter efficiency are analytically investigated and new optimum design rules are developed, and the results of the analysis are graphically displayed to point to a practically viable and an efficient design of the proposed converter.**

I. INTRODUCTION

In most power electronic applications, diode rectifiers with capacitive filtering are used in the front end of a power converter as an interface with the electric utility because they provide high power density, high efficiency, high reliability and low cost. However, the rectifiers draw large-amplitude short-duration spikes of current from the power line during the time intervals near the peaks of the voltage waveform. This current waveform has a large harmonic content, which causes voltage distortion and electromagnetic interference, unfavorably affecting other users of the power system. In addition, the increased harmonic currents result in increasing Volt-Ampere ratings of the utility equipment and more importantly cause the rectifier input to have a low power factor, which means inefficient use of electric energy.

For these reasons, high power factor has become a requirement in many ac/dc converter and power supply specifications. To reduce the unfavorable effects of the harmonic currents, utilities, governments and international agencies have imposed regulations to limit the harmonic content of the current drawn from the power line by these power electronic converters. Some of these regulations are IEEE Std. 519 [1], and the European Norm IEC 1000-3-2 [2].

As a consequence, the development of ac/dc converters that comply with the new regulations make this topic one of the most important areas of research in power electronics. The research in this field is still very active and engineers are currently looking for cost-effective solutions. A detailed review of the recent progress in topology, control, and design aspects in three-phase power factor correction (PFC) techniques is presented in [8]. Our research is based on the work presented in [3]-[6]. The lack of isolation and strong dependence of THD to the voltage gain between input and output have motivated using flyback transformers [4]-[5]. However, the need for two primary windings in the transformer is a drawback of the circuits proposed in [4] and [5]. Each winding is used only during one half-cycle of the source voltage, causing the current in primary windings to have a poor rms to average ratio suggesting an increase in winding size, volume and less utilization.

We propose a new three-phase ac/dc converter topology that provides a high power-quality interface to the utility, which is shown in Fig. 1. This circuit is a discontinuous-current mode flyback converter that is loosely based on the circuit proposed in [3]. This converter requires three switches, but the operation of the three phases is in parallel thereby resulting in a single conversion stage. The flyback converter, operated in discontinuous conduction mode, provides near-unity-power-factor at its power input. In addition, as an inexpensive high-power-factor rectifier suitable for power supplies at the 100 and 200 W level (operated as single phase), it is the most favored power converter topology [6]. The objective of this work is to develop the technology for the proposed converter to meet the high-power factor requirements and to serve the demand for an advanced high-power, inexpensive, efficient and small size ac/dc rectifier in the telecommunications market. It is a generally accepted idea by design engineers today that flyback based converters are not practical and not suitable for high power applications. We are however confident that we can apply this topology at 12.5 kW with satisfactory results. We are encouraged because of the recent developments in the switching device technology (high voltage IGBTs and MOSFETs), capacitor technology (film capacitors that replace the electrolytics) and the alternative design methods like transformer interleaving, converter interleaving, and using coaxial transformers.

0-7803-7404-5/02/$17.00 (c) 2002 IEEE

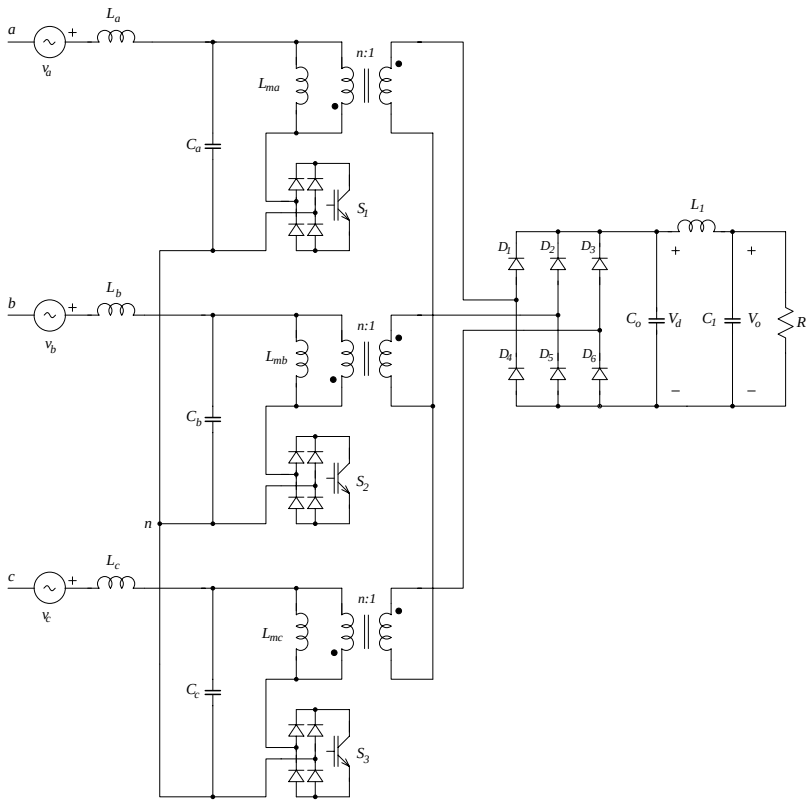


Figure 1: The proposed three-phase high power factor rectifier based on a flyback converter.

II. The Proposed Converter

Figure 1 shows the circuit topology of the proposed converter. As shown in Fig. 1, the inputs of the converter can be directly connected to a three-phase Δ or Y connected utility system through a low pass LC filter placed in each phase. The LC filter is used to remove the high frequency components of the input current. Since the voltages applied to the primary of the flyback transformers are ac waveforms, the controllable devices in series with the primaries have to support both polarities of voltage and current. Thus, the switches are placed in a full-wave diode bridge to create a bipolar switch, as shown in Fig. 1. In this case an IGBT is used as the controllable device. Since the currents transferred to the secondary also vary sinusoidally, a three-phase full wave rectifier bridge is required at the output of the converter.

III. Principles of Operation

The proposed topology uses three controllable switches that are switched at constant frequency and constant duty ratio. During each conduction interval of the controllable switch, the instantaneous value of the magnetizing current rises from zero to a peak value that is dictated by the instantaneous value of the source voltage for that phase. Specific current values during each on interval (Fig. 1) are proportional to the average value of their input phase voltages during the same on interval. Since the average value of each of these voltages varies sinusoidally, the input current peaks also vary sinusoidally. The fact that the current pulses always begin at zero suggests that their average values also vary sinusoidally. Consequently the input ac current consists of the fundamental (60 Hz) component and a band of high frequency unwanted components centered around the switching frequency (f_s) of the controllable switch. Since this switching frequency can be in the order of several tens of kilo-Hertz, filtering out the unwanted input current harmonics becomes a relatively easy task.

As the controllable switch is turned off, the magnetizing current is reset through the secondary winding. The currents transferred to the secondary are rectified and used to charge the output capacitor. Input power control (or the output voltage regulation) can be achieved through the transformer turns ratio and pulse width modulation of the controllable switch on interval at constant frequency (f_s).

IV. Analysis

Analysis is performed only for a single phase (phase *a*) since the operation of the three phases is in parallel. The worst operating point for the design of the converter is when the input voltage is at its maximum and the output voltage is minimum. Thus, the analyses and the design decisions are made for the switching interval that coincides turning on the switches at the peak of the input voltage.

A. Analysis When the Switches are Closed

Figure 2 shows the equivalent circuit of the topological stage when all three switches S_1, S_2 and S_3 are turned on. The bold lines display the active parts of the circuit and the current flow within the topology. Because the output rectifiers (D_1 through D_6) are all reversed biased during the on time of the switches, there will be no current flow to the secondary leaving the current flow only in the primary side of the converter. In addition, since a balanced system is assumed, the voltage of the secondary neutral point is at the mid-potential of the output voltage. A fictitious connection that ties the secondary neutral point to the mid point of the output capacitor is provided in Fig. 2 in order to simplify the analysis.

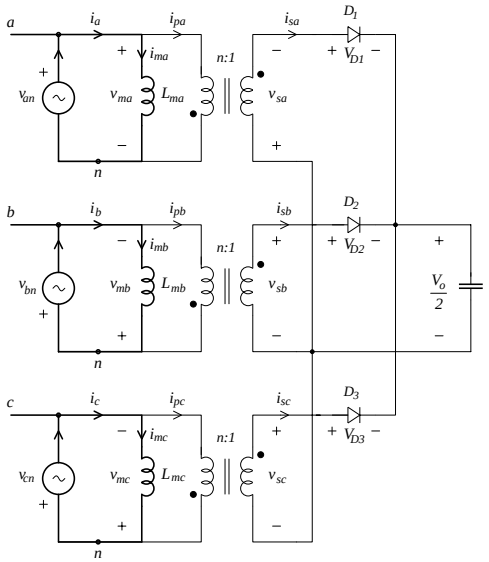


Figure 2: Equivalent circuit of the topological stage when the switches are closed, assuming v_{an} is positive, v_{bn} and v_{cn} are negative.

When the switch is turned on, the magnetizing current of phase *a* (i_{ma}) starts from zero and increases linearly with a slope of v_{an}/L_{ma}. The expression for the magnetizing current is given by

$$i_{ma}(t) = \frac{v_{an}}{L_{ma}} t . \tag{1}$$

At the end of the switch on time (DT), $i_{ma}(t)$ will have risen to a peak of

$$I_{ma,\,pk} = \frac{v_{an} DT}{L_{ma}}, \tag{2}$$

where $v_{an} = V\sin(\omega t)$ is the instantaneous source voltage and is assumed to be constant during the switching interval. Therefore, (2) becomes

$$I_{ma,\,pk} = \frac{V\sin(\omega t) DT}{L_{ma}} . \tag{3}$$

Equation 3 suggests that the peak of the magnetizing current occurring in a switching instant will change according to the instantaneous value of source voltage. Since the source voltage is a sinusoidal waveform, then the peaks of the magnetizing current will vary sinusoidally and follow a sinusoidal envelope, which is shown as the dotted line in Fig. 3. The current waveforms shown in Fig. 3 are conceptual waveforms and do not represent any actual results.

The sinusoidal envelope shown in Fig. 3 can be represented by the following expression

$$I_{ma,\,pk}(\omega t) = I_{pk}\sin(\omega t), \tag{4}$$

where I_{pk} represents the peak magnetizing current when phase *a* voltage is peaking and found by substituting $\pi/2$ for ωt in (3). Hence,

$$I_{pk} = I_{ma,\,pk}(\omega t) = \frac{VDT}{L_{ma}} \text{ at } \omega t = \frac{\pi}{2} . \tag{5}$$

B. Input Current Analysis

We know from the preceding analysis that the converter draws current from the input only during the time interval when the switches are closed. Therefore, the input current in phase *a* (i_a), for example, is equal to the magnetizing current ($i_a = i_{ma}$) during the D phase and zero for the remainder of the switching period. The solid line in Fig. 3 represents the conceptual input current waveform over the line cycle. The LC filter at the converter input removes the high frequency content of the input current by averaging the waveform.

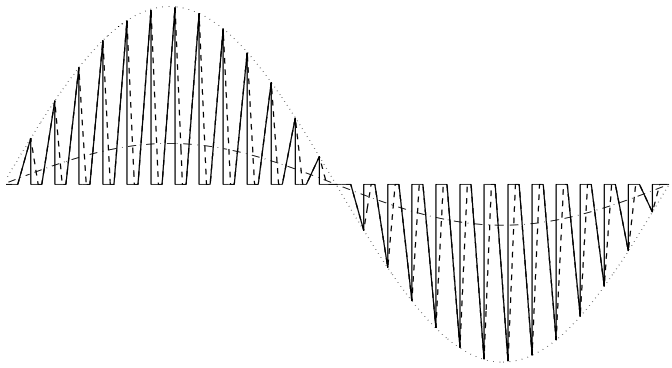


Figure 3: Conceptual current waveforms: solid line is the conceptual magnetizing (input) current during D phase, dash-dot line is the instantaneous average input current, dashed line is the magnetizing current during the off time of the switch, and dotted line is the magnetizing current peak envelope.

The switching cycle average of the input current is equal to the area of the triangle divided by the switching period and given by

$$I_{a,\,avg}(\omega t) \;=\; \frac{1}{T}\cdot\left(\frac{1}{2}\cdot DT\cdot I_{a,\,pk}(\omega t)\right), \tag{6}$$

where (ωt) is included to indicate a specific switching instant over the line cycle. Substituting $I_{pk}\sin\omega t$ from (4) for $I_{a,\,pk}(\omega t)$ in (6) yields

$$I_{a,\,avg}(\omega t) \;=\; \frac{1}{2}DI_{pk}\sin\omega t, \tag{7}$$

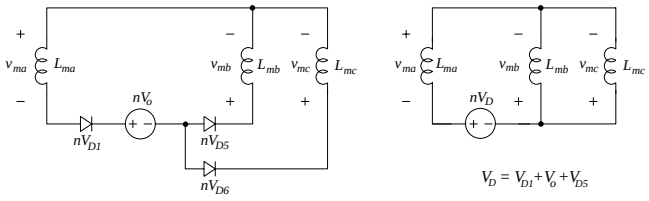
and using $\dfrac{VDT}{L_{ma}}$ for I_{pk} gives the analytical expression for the instantaneous average input current as

$$I_{a,\,avg}(\omega t) \;=\; \frac{VD^2T}{2L_{ma}}\sin\omega t. \tag{8}$$

Equation 8 reveals important information about the operation of the converter, which is how a high power factor is achieved. As mentioned before, the converter is operated at constant switching frequency and constant duty ratio over the entire line cycle. This condition suggests that all the parameters in (8) except the $\sin(\omega t)$ term are constants. Therefore, it is concluded that the instantaneous average of the input current (i_a) is sinusoidal and in phase with the input voltage, which is shown in Fig. 3 as the dash-dot line.

C. Analysis When the Switches are Open

After the switches turn off, the sudden interruption of the current in the magnetizing inductors forces the transformer voltage to reverse in an attempt to keep the flux constant. The reverse voltage across the magnetizing inductances rises very quickly until the appropriate output rectifiers conduct. For example, due to the relative polarity of the input voltages considered in this analysis, the rectifiers D_1, D_5 and D_6 in Fig. 1 will turn on. The equivalent circuit for this topological stage is shown in Fig. 4. Conduction of these rectifiers provides a circulating path for the magnetizing currents of each phase and clamps the rising voltage across the magnetizing inductances to the flyback voltage (transferred output voltage). According to the equivalent circuit in Fig. 4b, two thirds of nV_D (n is the turns ratio, V_D is the output voltage including the on state voltage of the rectifiers) appears across the primary of phase *a* and one third appears across the primary of phases *b* and *c*, assuming a balanced system. Consequently, these negative voltages are used to reset the current in the magnetizing inductances of the three phases, the conceptual magnetizing current for phase *a* during this interval is shown as the dashed line in Fig. 3. Moreover, the turns ratio of the transformers is adjusted so that converter always operates in discontinuous current mode.



(a) (b)

Figure 4: Equivalent circuit for the topological stage when the switches are open, assuming v_{an} is positive, v_{bn} and v_{cn} are negative.

V. DESIGN

The specifications used in the design of the proof-of-concept converter are listed in Table I.

TABLE I: THE DESIGN SPECIFICATIONS FOR THE CONVERTER.

Input voltage	480 V rms (nominal, line to line)
Output voltage (V_o)	45 V-58 V dc
Ripple factor (R_c)	0.0025
Maximum output power (P_o)	12.5 kW
Efficiency	90%
Three phase input power	13.89 kW
Maximum output current	215 A

Based on the developed analytical design rules and simulation results, the optimum design parameters for the proof-of-concept converter are found as:

Switching frequency, f_s : 50 kHz
Magnetizing inductance, L_m : 43 µH
Maximum duty ratio, D_{max} : 0.57
Transformer turns ratio, n : 22
Primary peak current, I_{pk} : 92.8 A
Output capacitance, C_o : 1300 µF

The list of components used in the prototype converter are listed in Table II.

TABLE II: THE COMPONENTS USED IN THE PROTOTYPE CONVERTER.

Controllable device	Semikron 1700 V NPT IGBT, SKM300173D
Diodes for the bipolar switch	IXYS 1200 V Hiperfast Diodes, DSEI 2x61-12A, two diodes are in series
Output capacitor	Film capacitors, Electronic Concepts, Inc., UL30AR0660
Output rectifiers	International Rectifier 100V, 200A Schottky diode, 203DMQ100
IGBT gate drive	Hewlett Packard's IGBT gate drive, HCPL-J312, followed by another high speed current booster circuit.

VI. Experimental Results

The prototype converter was tested under hard-switching conditions, except for the clamp circuits that are used to protect the IGBTs from overvoltages. As we stated before, the peaks of the magnetizing current follow a sinewave envelope as seen in Fig. 5. Figure 6 shows the expanded view of the magnetizing current and when operating at 50% duty ratio. This is at the same time the current drawn from the input before filtering. Figure 7 shows the same magnetizing current after filtering, which is the input phase current, and the input line to neutral voltage. The current waveform in Fig. 7 clearly shows that all the high frequency components are successfully removed and a small THD is achieved. The distortion appearing near the peak of the voltage and the current waveforms is coming from the utility side not from the converter. The same distortion was observed even when the converter is not operated.

A set of test results obtained from the proof-of-concept converter for a particular set of input and output parameters is displayed in Table III. The current waveform shown in Fig. 7 and the test results given in Table III demonstrate the ability of the proposed converter to draw perfectly sinusoidal currents from the utility, and thus providing high power-quality interface to the power network while supplying the load. However, the efficiency of the converter measured less than expected, 50.5%. Prior to the experiment, we analytically calculated the theoretical efficiency of the prototype converter as 80% at full load. And the fact that the power lost in the clamp circuits are measured to be around 30% of the input power revealed that the leakage and the parasitic inductances are significantly affecting the energy transfer in the converter. Analysis of the converter with leakage inductance has shown that the leakage inductance delays the transfer of the primary current to the secondary, thus preventing a substantial portion of the magnetizing energy from transferring to the output and diverting it to the clamp instead. A detailed discussion about this problem is given in the next section.

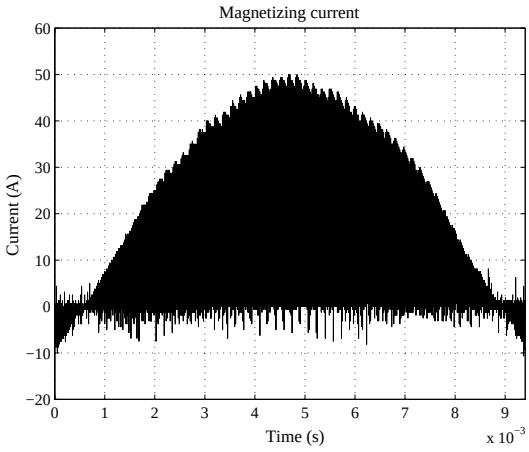


Figure 5: Transformer magnetizing current over one half of a line cycle.

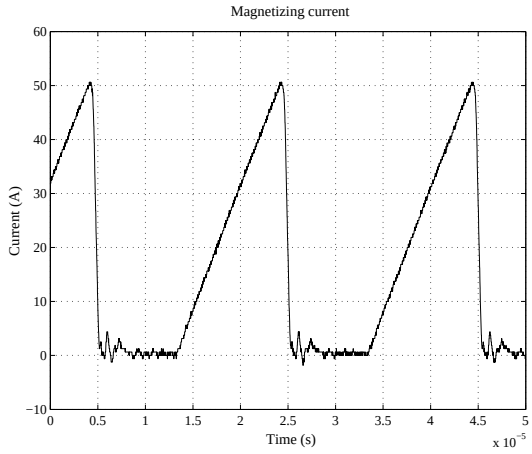


Figure 6: Switching cycle details of the transformer magnetizing current.

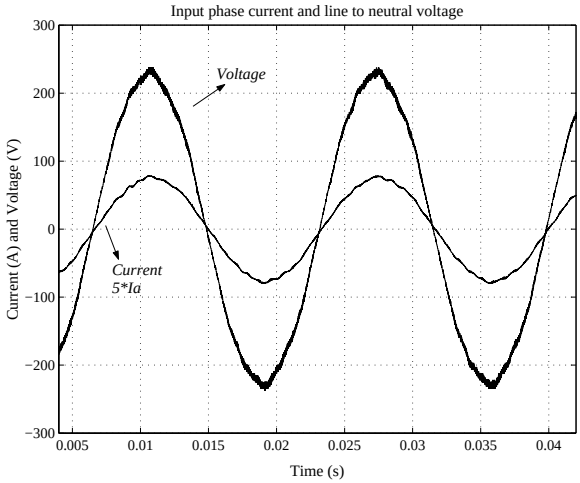


Figure 7: Input phase current and line to neutral voltage.

TABLE III: Experimental test results.

Parameter	**Measured data**
Input voltage and current	159 V rms, 10.8 A rms
Input power	5151.6 W (Total three-phase)
Output power	2600 W
Efficiency	50.5%
THD of the input current	2.5% (THD of the source voltage is 2%)
Input power factor	0.991

VII. Adverse effects of the leakage and parasitic inductances on the energy transfer of the proposed converter to the output

As also seen from the experimental results, the transformer leakage and the parasitic inductances are the largest factors in degrading the performance of the proposed converter. As we know, in a discontinuous mode flyback converter, the energy stored in the flyback transformer must be zero at the begin-

ning and end of each switching period. During the "on" time of the switch, energy taken from the input is stored in the transformer. When the switching device turns off, all of this stored energy is delivered somewhere – ideally to the output. However, the transformer leakage and parasitic inductances cause much of the stored energy to be dumped into the primary side snubber or clamp, diverting it from the output. These inductances dump not only their own energy, but also cause much of the energy stored in the mutual inductance to be diverted into clamp circuits. That is why the prototype converter suffers from poor energy transfer to the output and low efficiency. A more detailed discussion about this problem can be found in references [7] and [9]-[11].

This situation gets worse at high power levels and at high switching frequencies because the demand for high input power at high frequencies requires very small values of magnetizing inductance. As a result, the ratio of leakage and parasitic inductances to the magnetizing inductance tends to be higher. The increase in the relative magnitude has an important effect on the power transfer of the converter.

Based on the developed idealized analytical models that characterize the current transfer process at turn-off with leakage inductance, we derived a closed-form equation in which we relate the efficiency of the converter to the transformer leakage and parasitic inductances (series inductance, L_s) in a quantitative manner [7]. The derived equation was then used to construct the efficiency curves for different values of series inductances and clamp voltages, which are shown in Fig. 8. The solid curve in Fig. 8 represents the efficiency variation for the ideal case without the clamp. The dashed curve represents the efficiency when the switches (IGBTs) are clamped at 1500 V. The area above the solid curve indicates the energy loss due to only the series inductances in the ideal case. The area between the solid curve and the dashed curve represents the energy taken down to the clamp circuits from the energy stored in the mutual inductance because of the delay in current transfer. The delay is caused by the series inductance when the voltage across it is clamped. The dotted curve is the overall efficiency of the converter.

These curves show the strong dependence of the efficiency on the ratio of the series inductance to the magnetizing inductance, *k*, and to the clamp voltage. We measured 20% series inductance in the prototype converter. 8% of it is the transformer leakage inductance and 12% of it is the series parasitic inductances such as wiring inductance and internal inductances of the components particularly at the secondary side (assuming the leakage inductance is referred to the secondary). If we enter the efficiency curves at 0.2, we find an overall efficiency of 43% under hard switching along with 37% of the input power being stored in the clamp capacitor. This result shows why the prototype converter measured low efficiency. Since the converter stores substantial energy in the clamp capacitor, recovery of this much power is not practical.

Because the magnetizing inductance has to be very small for high power applications, the parasitic inductances become relatively large compared to it. Another disadvantage in this particular application is the requirement for a large turns ratio, $n = 22$, which ensures discontinuous mode operation for an output voltage of 40 V. To obtain a reasonable efficiency with the current design, according to the curves given in Fig. 8 the series inductance should be reduced to less than 5%. Some techniques such as using multilayer conductors, PCB connections and paralleling of the components can provide major reduction of parasitic inductances. However, 8% transformer leakage inductance and some additional parasitic inductance suggests a practical limit how small we can make the relative magnitude.

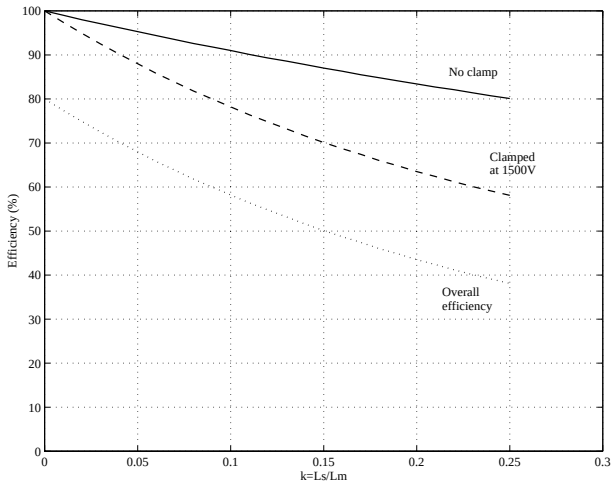


Figure 8: Variation of the analytically calculated efficiency of the proposed converter versus *k*, where $k = L_s / L_m$. The solid curve represents the ideal case without the clamp, the dashed curve is when the clamp voltage is 1500V and the dotted curve is the overall efficiency of the converter.

Nevertheless, if the current design and so the prototype is modified to support the applications that require higher output voltages, the output characteristic of the converter drastically improves and enables more efficient power conversion. For example, the turns ratio of the transformer can be halved, $n = 11$, for an application that requires 80 V and higher output voltage. Halving the turns ratio results in a four times larger magnetizing inductance at the secondary side, and correspondingly reduces the relative magnitude of the series inductances to the magnetizing inductance by a factor of four. Considering that the same leakage and parasitic inductances are present, the *k* factor then becomes 0.05. Moreover, application of techniques described above to reduce the parasitic inductances will further reduce *k* to a value less than 5%. As seen from Fig. 8, for example, 4% series inductance results in 70% efficiency under hard switching and causes 10% of input power to be stored in the clamp circuits. Transferring the energy from the clamps to the output using energy recovery

converters can bring the efficiency to near 80%. Soft switching of IGBTs along with the energy recovery can further improve the efficiency to more than 80%. The experimental results of this new design alternative is presented in the next section.

VIII. Test Results with The Modified Design

With the modified design, the turns ratio is changed from previous value of 22 to 11. The transformer in the original design had interleaved windings, that is, the primary is sandwiched between the two secondaries in order to reduce the leakage inductance. With the modified design, the two secondary windings are connected in series to achieve doubling of the number of turns. The rest of the experimental setup remained unchanged. During this experimental evaluation, a stand alone three-phase ac source was used instead of the utility grid. A set of test results obtained from the modified experimental converter is shown in Table IV.

The data presented in Table IV clearly shows the viability of the modified design. As expected, the efficiency and the power transfer capability of the converter is significantly improved. The efficiency under hard switching case is 70.94%, which was expected based on the curves in Fig. 8. Moreover, both THD and power factor are also improved because of the voltage quality of the ac source used in the experiment. The waveforms of the input line to neutral voltage and the phase current for the modified design are shown in Fig. 9. The phase shift between the voltage and current is caused by the LC filter at the input.

TABLE IV: Experimental test results with the modified design.

Parameter	**Measured data**
Input voltage Input current	208 V rms (line to neutral) 16.4 A rms
Input power	10233.6 W (Total three-phase)
Output power	7260 W
Efficiency	70.94%
THD of the input current	1%
Input power factor	0.9972

IX. Conclusions

This paper has presented a new three-phase high power-quality utility interface system. The proposed converter particularly was designed to serve the need for an advanced 12.5 kW high power-factor ac/dc converter in the telecommunications market. Experimental results showed that the converter achieves near-unity power-factor and output voltage regulation in a single stage. However, the efficiency measured lower than expected. Further study revealed that parasitic inductances significantly affect the energy transfer to the output. Motivated by this problem, new idealized analytical models were developed to study the current transfer process at turn-off. Finally, a set of design curves was derived to select the most practical design for the proposed converter. A new design alternative was introduced and discussed. A flyback converter topology is first time implemented in very high-power application. The results of this study will provide a strong basis for the future developments for the proposed converter because of the promising recent developments in high voltage switching device technology.

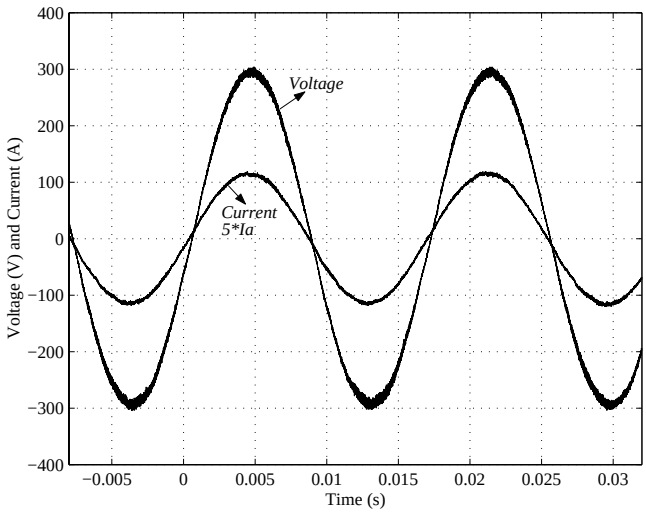


Figure 9: Input line to neutral voltage and phase current with the modified design.

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A Novel Three-Phase Utility Interface Minimizing Line Current Harmonics of High-Power Telecommunications Rectifier Modules

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***Abstract*— Based on the combination of a three-phase diode bridge and a dc/dc boost converter, a new three-phase three-switch three-level pulsewidth modulated (PWM) rectifier system is developed. It can be characterized by sinusoidal mains current consumption, controlled output voltage, and low-blocking voltage stress on the power transistors. The application could be, e.g., for feeding the dc link of a telecommunications power supply module. The stationary operational behavior, the control of the mains currents, and the control of the output voltage are analyzed. Finally, the stresses on the system components are determined by digital simulation and compared to the stresses in a conventional six-switch two-level PWM rectifier system.**

***Index Terms*— Comparison of converter concepts, control of neutral point potential, hysteresis control of mains phase currents, neutral-point-clamped converter, three-phase three-level PWM rectifier (VIENNA rectifier).**

I. Introduction

CONVENTIONAL power supplies of the interchanges of telecommunication systems are being replaced more and more by modular rectifier systems, due to the advantages of the latter concerning operational behavior, systems technology, and costs. There, the rectifier modules (having a three-phase supply for a higher number of subscribers and/or higher rated power) are realized as voltage dc-link converters in general. In the simplest case, the mains ac voltage is converted into a dc-link voltage by a three-phase diode bridge with capacitive smoothing. This dc-link voltage is then transformed into the output dc voltage by a high-frequency dc/dc converter connected in series.

The realization of the input stage of a power supply module as an uncontrolled three-phase bridge (in many cases directly connected to the mains) is motivated by the requirement of a high power density, high efficiency, high reliability (robustness), and low cost. However, this concept shows the disadvantage of high effects on the mains, due to high amplitudes of low-frequency mains current harmonics which lead to a distortion of the mains voltage. Therefore, the danger of an influence on, or disturbance of, other loads is present. This is true especially for high installed power and high inner mains impedance. In connection with the limitation of harmonics stress on the public low-voltage mains caused by power electronic converters—as requested by guidelines [1], recommendations, and future standards (IEEE Std. 519-1992, IEC-555-2, and IEC-555-4 [2])—the development of ac/dc converters having low influence on the mains is of special importance. This is especially important for guaranteeing universal applicability of telecommunication rectifier modules.

The scope of this paper is the development and analysis of a new three-phase high-frequency unidirectional pulsewidth modulated (PWM) ac/dc converter for feeding the dc link of a 12-kW telecommunications power supply module. For the determination of the circuit concept, the following basic requirements are given:

- approximately sinusoidal current consumption;
- resistive mains behavior;
- controlled output voltage;
- low-blocking voltage stress on the power transistors;
- high power density;
- high efficiency;
- low complexity of the power and control circuits;
- high reliability.

In Section II, the topology of a new three-phase three-switch three-level ac/dc boost converter is derived based on the basic structure of the power circuit of a three-phase ac/dc converter with controlled output voltage. This basic structure mentioned is based on the series connection of a three-phase diode bridge and a dc/dc boost converter. In Section III, the stationary operational behavior of the converter is analyzed. Based on this, the control range of the phase angle of the mains current is determined, as well as the minimum value of the output voltage being required for a given output power and given mains current phase angle for sinusoidal shape of the mains current. In Section IV, the tolerance band control (in order to have low development and production costs) of the mains current and the control of the capacitive center point of the output voltage (being included into the system function) are discussed. The realization of these considerations is discussed in Section V by using digital simulation. Finally, in Section VI, the voltage and current stresses on the active and passive components are given for

ouput power	12.6 kW;
output voltage	700 V;
mains line-to-line voltage	400 V;

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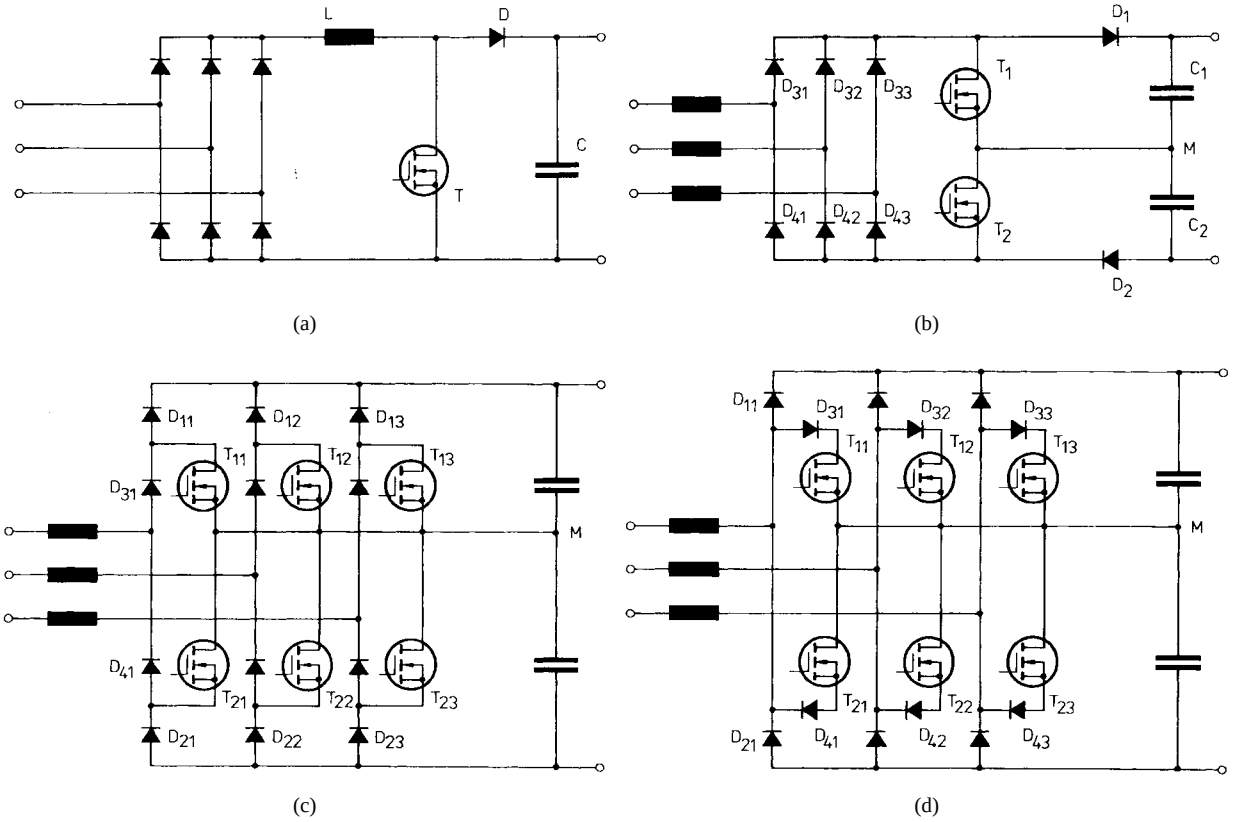


Fig. 1. Development of the basic circuit structures of three-phase three-level PWM rectifiers [(c) and (d)] based on a combination of a three-phase diode bridge and a dc/dc boost converter (a).

(there, one assumes that the system is applied for supplying the dc/dc converter part of a telecom power supply module with rated output power 12 kW (60 V/200 A) and efficiency of $\eta_{\mathrm{dc/dc}} \approx 0.95$). Also, a comparison is made to the component stresses of a conventional six-switch two-level voltage dc-link PWM rectifier system.

II. Derivation of the Circuit Structure

For the realization of a three-phase unidirectional ac/dc converter with controllable output voltage, a series connection of an uncontrolled diode bridge and a dc/dc boost converter can be used in the simplest case (Fig. 1(a), [4]). However, in the mains current spectrum of this system, low frequency harmonics of high amplitude are present. Due to the operating principle of a three-phase diode bridge, only two phases always conduct current (with the exception of the commutation intervals). Therefore, the phase current shape shows $\pi/3$-wide intervals with zero current.

A reduction of the effects on the mains of this system can be obtained by placing the inductor L on the ac side and by operating the converter in the discontinuous conduction mode (DCM) [6]. Analogous to the DCM of single-phase ac/dc boost converters [7], in this case, a voltage proportional guidance of the peak values of the discontinuous input currents is given directly by the mains phase voltages (for time constant duty cycle of the power transistor T). However, as a closer analysis of the system behavior shows, the harmonic content of the mains phase currents remaining after filtering of the discontinuous input quantities is essentially determined by the output voltage level [8]. A largely sinusoidal mains current shape is linked to an output voltage being large with respect to the amplitude of the line-to-line mains voltage. For operating the system with the European low voltage mains (nominal rms line-to-line voltage: 400 V) we, therefore, have to split up the dc-side converter part (due to the blocking voltage stress on the dc-side power semiconductors for an output voltage >1 kV) into two simultaneously pulsed partial systems (Fig. 1(b) or [9, Fig. 10]) having each to sustain half of the dc-link voltage.

The application of the circuit described so far is limited, especially by the discontinuous input current shape leading to high current stress on the power semiconductor devices and by the filtering effort required for limiting the conducted electromagnetic influence (EMI) [9]. These aspects exist in addition to to the high blocking voltage stress on the power semiconductor devices of a converter fed from the high dc-link voltage. Therefore, for the requirement of high output power, one has to ask the question for alternative concepts of three-phase unidirectional PWM boost rectifiers with continuous input current showing (ideally) purely sinusoidal shape and being independent of the output voltage level (being larger than the maximum value of the line-to-line mains voltage).

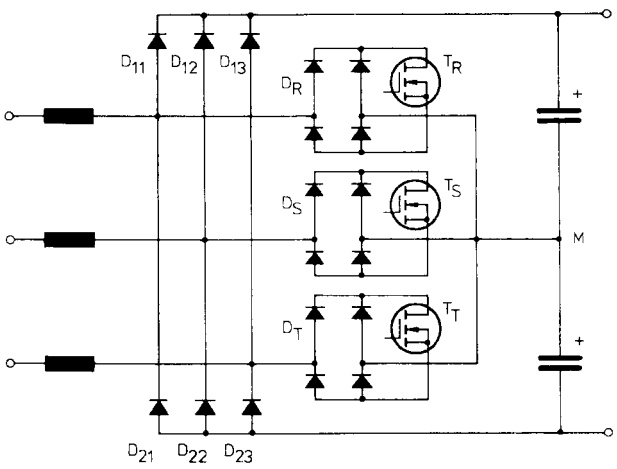
The current consumption of the system shown in Fig. 1(b) is defined, in general, by the difference between mains voltage and rectifier input voltage lying across the inductances connected in series at the input. A continuous, sinusoidal

mains current shape (with the exception of the harmonics with pulse frequency and their multiples), therefore, is obtained only by rectifier input voltages having sinusoidal shape in the average over the pulse periods. Therefore, this requires a separate controllability of the voltage synthesis of each phase or the application of synchronously controlled transistors T_{1j} and T_{2j} and of ouptput diodes D_{1j} and D_{2j} in each bridge leg $j = 1,2,3$, respectively [Fig. 1(c)]. Due to the inclusion of the center point of the output voltage into the system function, all power semiconductors of the resulting circuit (called *forced commutated three-phase boost-type rectifier* in [11]) only have to sustain half of the output voltage. However, the advantage of the low blocking voltage stress is followed by the disadvantage of relatively high conduction losses, because the entire current flow connected with supplying the output power goes through the diode legs due to the rectifier function of the converter.

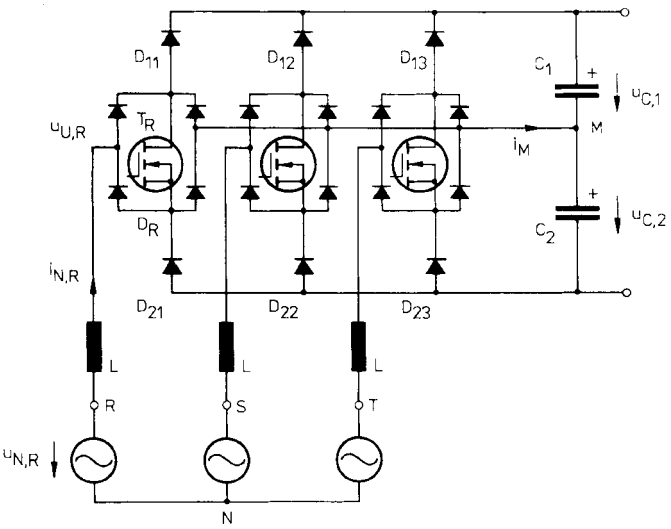
A reduction of the conduction losses can be obtained by shifting the diodes D_{3j} and D_{4j} into the circuit legs controlling the conduction state of the converter [Fig. 1(d)]. A further advantage of this circuit modification consists in the fact that then, in each phase, a bidirectional bipolar switch is realized by the control legs lying in antiparallel (D_{3j}, T_{1j} and T_{2j}, D_{4j}). This switch can be replaced, as shown in Fig. 2(a), by the combination of a single-phase diode bridge D_i and a power transistor T_i, $i = R,S,T$. Compared to a realization according to Fig. 1(c) or (d), this results in reducing the number of the turn-off power electronic devices by 50% and/or reduced control effort and in a higher utilization of the power transistors (there, the entire and not only half of the total transistor chip area of a phase is always used for conduction and control of the input current). However, now the diodes D_{1j} and D_{2j} have to sustain the full output voltage (and not, as for the circuit according to Fig. 1(c), only half of the output voltage) in the blocking direction. This disadvantage can be avoided, however, in a simple manner by the integration of the bidirectional bipolar switches T_i, D_i into the bridge legs of the diode bridge on the input side [19]. This results in a new converter topology [Fig. 2(b)] which will be called *three-phase three-switch three-level (three-phase/switch/level) PWM (VIENNA) rectifier* in the following. Its detailed analysis is the topic of this paper.

Remark: One has to mention that, regarding the circuits shown in Fig. 1(c) and (d), a close topological relationship exists to the basic types of three-phase three-level PWM *inverters* introduced in [12] and [13]. Furthermore, one has to point out a modified circuit realization proposed in [14] according to Fig. 1(c), a PWM inverter circuit being identical with Fig. 2(a) regarding the control leg realization (as analyzed in [15]), and a converter structure which can be derived by further development of the circuit according to Fig. 2(a) as described in [16] using low switching frequency, i.e., three times the mains frequency. Single-phase realizations of the circuits given in Fig. 2 are analyzed in [17] and [18].

For the sake of completeness, we finally want to bring attention to papers describing circuit concepts of three-switch *two-level* PWM rectifiers, e.g., [19], [20] (cf. pp. 87–89), and [21]–[23].



(a)



(b)

Fig. 2. Basic structures of novel three-phase/switch/level unity power factor PWM (VIENNA) rectifier systems resulting by further development of Fig. 1(d); the feeding mains is replaced by voltage sources $u_{N,i}, i = R,S,T$; N denotes the mains star point. The circuit shown in (b) has higher conduction losses as compared to the circuit according to (a). However, the diodes D_{1j} and D_{2j} (as well as all other power semiconductor devices) of (b) only have to sustain half of the output voltage. Due to the (in general) longer reverse recovery time of diodes with higher blocking voltage capability (and/or the higher switching losses connected herewith) one has to prefer circuit (b) for high pulse frequency as compared to (a).

III. Principle of Operation

A. Basic Function

For describing the basic function of the rectifier systems shown in Fig. 2, the analysis is limited to the fundamentals of the system quantities on the ac side.

Based on a single-phase equivalent circuit (Fig. 3), there follows (using complex ac current calculus) for the phasor of the rectifier input voltage fundamental [denoted by the index (1)]:

$$\underline{U}_{U,(1)} = \underline{U}_N - j\omega_N L \underline{I}_{N,(1)}. \tag{1}$$

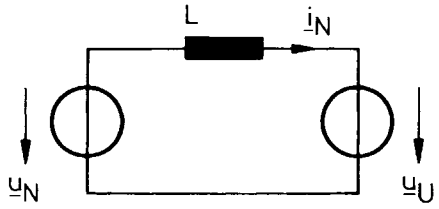


Fig. 3. Single-phase equivalent circuit related to the fundamental for the ac-side system section of a three-phase/switch/level PWM (VIENNA) rectifier.

The current consumption (and, therefore, the basis for the power consumption)

$$\underline{I}_{N,(1)} = \hat{I}_{N,(1)} \exp j(\varphi_N - \varphi) \tag{2}$$

$(\varphi_N = \omega_N t)$ of the system is defined by the voltage lying across the inductances L connected in series on the ac side. There, this voltage is the difference between the (sinusoidal) mains voltage

$$\underline{U}_N = \hat{U}_N \exp j\varphi_N \tag{3}$$

$(\underline{U}_N = \underline{U}_{N,(1)})$ and the rectifier input voltage fundamental $\underline{U}_{U,(1)}$ which can be controlled regarding amplitude and phase via appropriate pulsation of the power transistors T_i, $i = R, S, T$ (Sections III-B and IV-A).

The power delivered to the dc side follows (if the system losses are neglected), based on the power balance, as

$$P_O = U_O I_O = \tfrac{3}{2} \hat{U}_N \hat{I}_{N,(1)} \cos\varphi. \tag{4}$$

B. Rectifier Input Voltage

Forming of a rectifier input phase voltage $u_{U,i}$ is influenced according to

$$u_{U,i} = \begin{cases} \operatorname{sign}\{i_{N,i}\} \dfrac{U_O}{2} & \text{if } s_i = 0 \\ 0 & \text{if } s_i = 1 \end{cases} \tag{5}$$

also by the sign (direction) of the associated mains phase current $i_{N,i}$, besides by the switching state of the power transistor T_i defined by a binary switching function s_i. (As reference point of the voltage $u_{U,i}$ the center point M of the dc-link voltage is chosen.) Each brigde leg shows a three-level characteristic, i.e., three possible voltage values $+(U_O/2)$, 0, and $-(U_O/2)$. Accordingly, the system is called a *three-level PWM rectifier*.

C. Stationary Operating Region

Due to the influence on the voltage generation caused by the sign of the phase currents [see (5)], the stationary maximum amplitude of the rectifier input voltage fundamental $\hat{U}_{U,(1),\max}$ (how it can be obtained without overmodulation) is defined also by the phase difference between $\underline{U}_{U,(1)}$ and the mains current fundamental $\underline{I}_{N,(1)}$. This definition by the phase difference has to be seen, besides the control limit $\hat{U}_{U,(1),\max} \leq (1/\sqrt{3})U_O$, which is given basically for bridge circuits. Therefore, in general, the definition of $\underline{U}_{U,(1)}$ is equivalent to defining the operating region of the converter [see (1)].

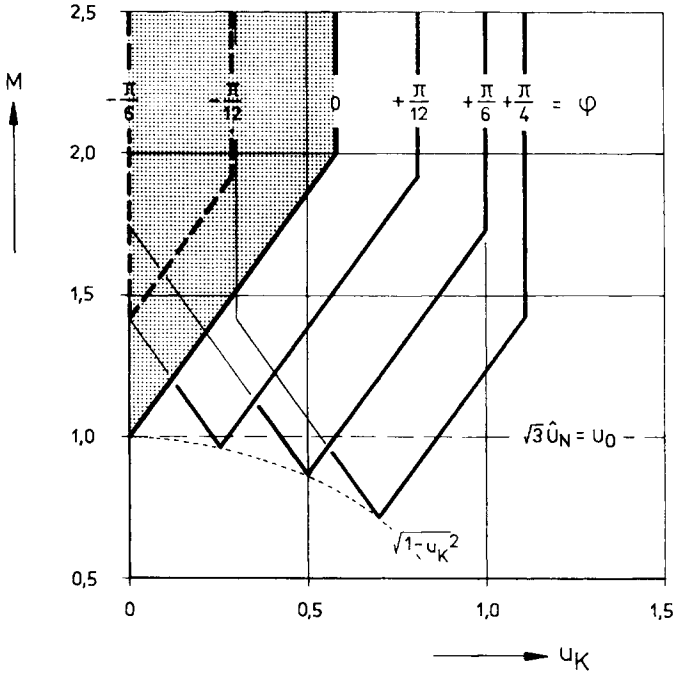


Fig. 4. Dependency of the operating region of a three-phase/switch/ level PWM rectifier system on the phase angle φ of the mains current (representation limited to angles within the interval $\varphi \in [-(\pi/6), +(\pi/4)]$ for the sake of clarity). The limits of the operating regions are show by solid lines for $\varphi > 0$., and for $\varphi < 0$, dashed lines are used. The operation region for resistive mains fundamental behavior $(\varphi = 0)$ is marked by the dotted area.

For the case of a resistive mains fundamental behavior [$\varphi = 0$, (2)], being important for practical applications, the operating region of the PWM rectifier system is determined by

$$u_K \leq \begin{cases} \dfrac{1}{\sqrt{3}}(M-1) & \text{if } M \leq 2 \\ \dfrac{1}{\sqrt{3}} & \text{if } M > 2 \end{cases} \tag{6}$$

where

$$u_K = \frac{1}{\hat{U}_N} \hat{I}_{N,(1)} \omega_N L \tag{7}$$

characterizes the load condition of the converter and where

$$M = \frac{U_O}{\sqrt{3}\hat{U}_N} \tag{8}$$

defines the system voltage transformation. Because for high pulse frequency of the system there is always $u_K \ll 1$ (typically $u_K \approx 0.01 \cdots 0.02$), only the limitation for $M \leq 2$ is of importance in (6). For the minimum value of the output voltage there follows, accordingly,

$$U_O \geq \sqrt{3}\hat{U}_N + 3\hat{I}_{N,(1),\max} \omega_N L. \tag{9}$$

Remark: For deriving (6), a description of the system operation based on complex three-phase phasors (complex space vectors) is advantageous, due to special clarity and a simpler calculation [24] as compared to a calculation with phase quantities. The analysis (not shown in detail here for

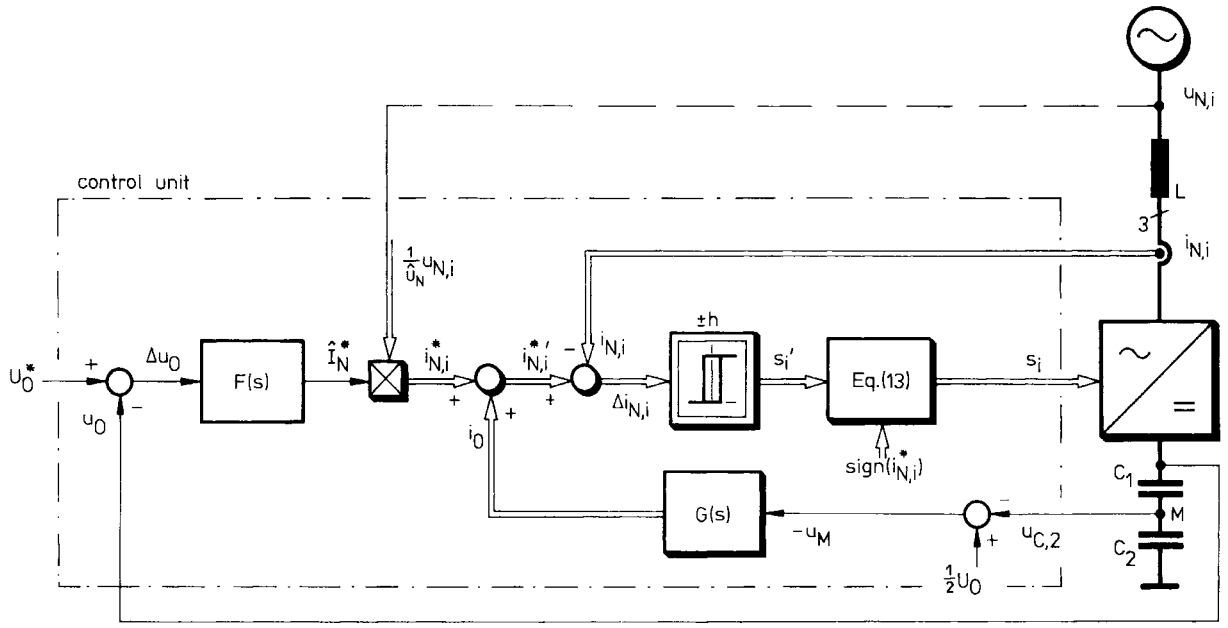


Fig. 5. Multiloop control of a three-phase/switch/level PWM (VIENNA) rectifier system. Outer control loops: $F(s)$: control of the output voltage u_O; $G(s)$: balancing of the output partial voltages $u_{C,1}$ and $u_{C,2}$. Inner control loop: tolerance band (or hysteresis) control of the phase currents $i_{N,i}, i = R, S, T$. The switching decisions s_i' of the hysteresis controllers are inverted according to (13) for $\operatorname{sign}(i^*_{N,i}) = -1$; for the sake of clarity, signal paths equivalent for all phases are combined into double lines.

the sake of brevity) also shows a basic restriction

$$-\frac{\pi}{6} \leq \varphi \leq \frac{\pi}{2} \tag{10}$$

of the operation of the rectifier system with inductive $(\varphi > 0)$ or capacitive phase angle of the mains current. According to Fig. 4, $\varphi = -(\pi/6)$ is only obtained there for $u_K \to 0$ or for $\hat{I}_{N,(1)} \to 0$ and, therefore, it constitutes only a theoretical limiting case. The real power transferred to the output circuit

$$P_O = \frac{3}{2}\frac{\hat{U}_N^2}{\omega_N L} u_K \cos\varphi \tag{11}$$

becomes zero at both limits of the operating region. Feeding back of energy from the output circuit into the mains $(\varphi \in (\pi/2, \pi]$ or $\varphi \in (-\pi, -(\pi/2))$, therefore, is not possible, as can also be seen immediately from the circuit structure (Fig. 2).

System operation with a capacitive phase angle, in general, is linked to a higher amplitude of the rectifier input voltage as compared to inductive mains behavior. This can be explained based on a phasor diagram. This also means that a higher value of the dc-link voltage and/or a higher voltage transformation ratio M is involved (Fig. 4).

Due to the dependency of the system control region on the phase difference of the fundamental of the rectifier input voltage and of the mains current, the minimum value $M_{\min}$ to be maintained for $u_K \to 0$ for capacitive *and* inductive mains current phase angle φ lies above the value $M_{\min} = 1$, which is given for resistive mains behavior. For inductive mains behavior, the output voltage U_O can theoretically be lowered in a section of the operating region below the voltage value $U_O = \sqrt{3}\hat{U}_N$ (and/or $M = 1$), resulting in the case of no-load and uncontrolled rectification $(s_i = 0)$. $\varphi \geq \pi/6$ requires a minimum load $u_K > 0$ of the system and is, therefore, of little practical importance.

IV. System Control

Besides a control of the mains current and of the output voltage, we also have to provide a control of the potential of the output voltage center point (and/or an active symmetrization of the output partial voltages) for the proposed system. This would not be required for conventional PWM rectifier systems, but requires only a minor additional circuit effort, as will be shown in the following.

A. Mains Current Control

The control of the power transistors and/or of the rectifier input voltage synthesis can be performed, in the simplest case, by a tolerance band or hysteresis control of the phase currents by independent phase current controllers.

The amplitude $\hat{I}_N^*$ of the phase current reference values

$$i_{N,i}^{*\prime} = \hat{I}_N^* \frac{u_{N,i}}{\hat{U}_N} \tag{12}$$

(which are derived directly from the phase voltages for resistive mains behavior) is given there by an output voltage controller $F(s)$, which is superimposed on the current control loop (Fig. 5). Because the control of the output voltage has no special features as compared to conventional converter systems, detailed explanations are omitted here for the sake of brevity.

The dependency of the sign of a rectifier input phase voltage $u_{U,i}$ (formed for $s_i = 0$) on the sign of the associated phase current $i_{N,i}$ [see (5)] has to be considered by generating the

control signals s_i of the power transistors by an inversion

$$s_i = \begin{cases} s_i' & \text{if } i_{N,i}^* \geq 0 \\ \text{NOT } s_i' & \text{if } i_{N,i}^* < 0 \end{cases} \tag{13}$$

(as controlled by the sign of the mains current reference value $\text{sign}\{i_{N,i}^*\}$, Fig. 5) of the switching decision

$$s_i' = \frac{1}{2}\left(1 + \text{sign}\left\{\Delta i_{N,i} - h\,\text{sign}\left\{\frac{d\Delta i_{N,i}}{dt}\right\}\right\}\right) \tag{14}$$

($\Delta i_{N,i} = i_{N,i}^* - i_{N,i}$ denotes the control error of the respective phase current $i_{N,i}$) of the associated tolerance band controller.

Remark: Equation (14) is valid for the assumption that $d\Delta i_{N,i}/dt$ does not change its sign within the tolerance band $|\Delta i_{N,i}| < h$. For $|\Delta i_{N,i}| > h$ the switching decision is independent of the cicuit/switching history and/or of the direction of the change of $\Delta i_{N,i}$. Then, (14) can be replaced by

$$s_i' = \begin{cases} 0 & \text{if } i_{N,i} > i_{N,i}^* + h \\ 1 & \text{if } i_{N,i} < i_{N,i}^* - h. \end{cases} \tag{15}$$

As already explained in Section III-A, the mains current consumption of the PWM rectifier system is defined by the voltage lying across the series inductances L

$$L\frac{di_{N,i}}{dt} = u_{N,i} - (u_{U,i} - u_N) \qquad i = R,S,T. \tag{16}$$

There, via the voltage of the floating mains star point N [see Fig. 2(b)]

$$u_N = \tfrac{1}{3}\sum_{i=R,S,T} u_{U,i} \tag{17}$$

which is influenced by the switching states of all phases, a coupling of the phase current changes is given. If independent phase current controllers are used, this coupling leads to the occurrence of limit cycles [27] and, therefore, to a nonoptimal utilization of the converter pulse frequency. Furthermore, the control error is not restricted to the deadband width h; the maximum value of the phase current ripple is defined by twice the value of the deadband width.

An avoidance of the disadvantages mentioned can be achieved by coordinating the switching actions of the phase current controllers [25]–[27]. This shall not be explained here in detail for the sake of brevity.

B. Balancing of the Output Partial Voltages

As mentioned before, besides control of the output voltage and of the mains phase currents, a symmetrical split

$$u_{C,1} = u_{C,2} = \frac{U_O}{2} \tag{18}$$

of the output voltage has to be guaranteed by the control system of the converter. An unsymmetry of the output capacitor voltages $u_{C,1}$ and $u_{C,2}$ (caused by loading the capacitive center point M by a dc current or low-frequency ac current) may be characterized by the voltage

$$u_M = \tfrac{1}{2}(u_{C,2} - u_{C,1}) \tag{19}$$

referred to the ficticious (ideal) center point of the output voltage. This unsymmetry will cause an increased voltage stress on one output capacitor, an increased blocking voltage stress on the power semiconductor devices situated in the control legs and on the freewheeling diodes of one bridge half, and an uneven current stress on the components over the fundamental period. According to (19), an ideally symmetric split of the output voltage is given for $u_M = 0$.

TABLE I
CENTER POINT CURRENT i_M AND VARIATION OF THE CENTER POINT POTENTIAL u_M IN DEPENDENCY ON THE CONVERTER SWITCHING STATE FOR $\varphi_N \in (-(\pi/6), +(\pi/6))$ OR $i_{N,R} > 0, i_{N,S} < 0, i_{N,T} < 0$ $(i_{N,R} \geq |i_{N,S}|, |i_{N,T}|)$, RESPECTIVELY [SEE (22)]; $(du_M/dt)_{\text{avg}}$ CHARACTERIZES THE POTENTIAL SHIFTS CAUSED BY A SWITCHING STATE BASED ON A RELATIVE ON-TIME BEING EQUAL FOR EACH SWITCHING STATE (s_R, s_S, s_T) AND BEING CONSTANT OVER φ_N; FURTHER ASSUMPTIONS: PURELY SINUSOIDAL MAINS CURRENT SHAPE AND HIGH, TIME CONSTANT PULSE FREQUENCY

s_R	s_S	s_T	i_M	$\left(\frac{du_M}{dt}\right)_{\text{avg}}$
0	0	0	0	0
0	0	1	i_T	−
0	1	0	i_S	−
0	1	1	$-i_R$	−−
1	0	0	$+i_R$	++
1	0	1	$-i_S$	+
1	1	0	$-i_T$	+
1	1	1	0	0

The current

$$i_M = \sum_{i=R,S,T} s_i i_{N,i} \tag{20}$$

loading the capacitive center point is formed by segments of the phase currents in dependency on the switching states s_i of the power transistors T_i. For the voltage shift of the center point there follows with $C_1 = C_2 = C$ (see Fig. 2):

$$\frac{du_M}{dt} = \frac{1}{2C} i_M. \tag{21}$$

For a clear description of the behavior in the following, a purely sinusoidal and symmetrical shape of the mains phase currents

$$\begin{aligned} i_{N,R} &= \hat{I}_N^* \cos(\varphi_N) \\ i_{N,S} &= \hat{I}_N^* \cos\left(\varphi_N - \frac{2\pi}{3}\right) \\ i_{N,T} &= \hat{I}_N^* \cos\left(\varphi_N + \frac{2\pi}{3}\right) \end{aligned} \tag{22}$$

and/or $i_{N,i} = i_{N,i}^*$ is assumed. Also, the analysis of the (stationary) operation is limited to an interval of the mains period $\varphi_N \in (-(\pi/6), +(\pi/6))$ and/or $i_{N,R} > 0, i_{N,S} < 0$, and $i_{N,T} < 0$ $(i_{N,R} \geq |i_{N,S}|, |i_{N,T}|)$. Due to the phase-symmetrical circuit structure, this includes the basic relationships within the entire mains period.

The center point currents i_M [see (20)] resulting for the possible combinations of the phase switching functions s_i (the different switching states of the converter, see Fig. 6) are given in Table I.

As described already in Section IV-A, a mutual influence of the phase current controllers is given due to the floating output

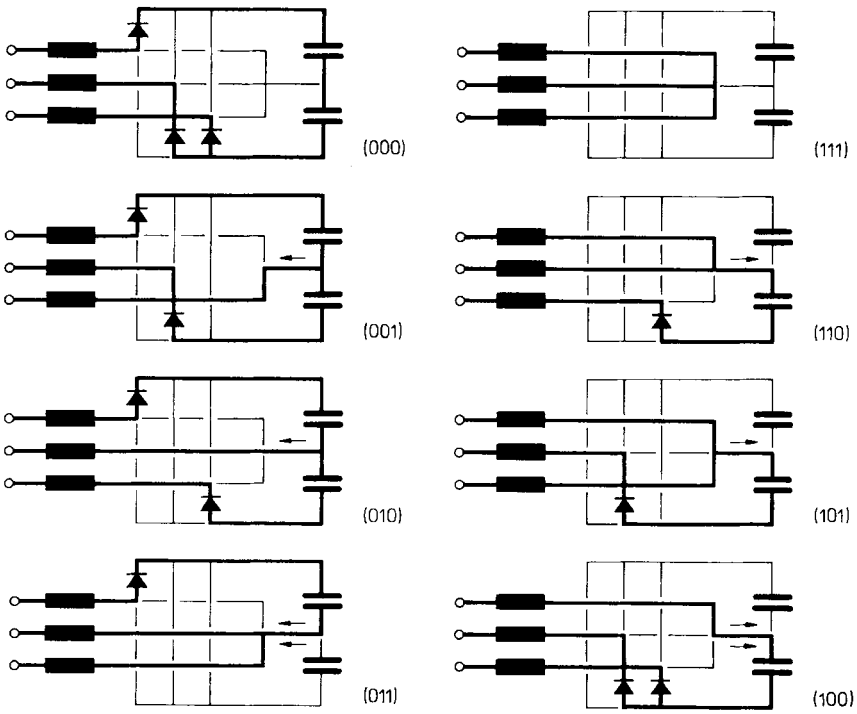


Fig. 6. Basis for the determination of the center point current i_M in dependency on the converter switching state (marked by (s_R, s_S, s_T)) for $\varphi_N \in (-(\pi/6), +(\pi/6))$ and/or $i_{N,R} > 0, i_{N,S} < 0$, and $i_{N,T} < 0$ $(i_{N,R} \geq |i_{N,S}|, |i_{N,T}|)$.

voltage center point M for independent hysteresis control of the phase currents; this leads to an arbitrary sequence and to a very variable duration of the single converter switching states (s_R, s_S, s_T). It is clear from the weighting of the switching states regarding the influence of the center point potential (see Table I) that one cannot expect a time constant average value of the center point voltage U_M (gained by averaging u_M over the mains period). This is also true because, as a closer analysis shows, for hysteresis control of the phase currents, a positive feedback effect occurs; an unsymmetry U_M of the output voltage leads to the occurrence of a current mean value (related to the fundamental period)

$$I_M = g_M U_M \qquad g_M > 0 \tag{23}$$

(being in a first approximation proportional to the unsymmetry U_M) increasing the unsymmetry. (The differential conductance $g_M > 0$ corresponds to the positive rate of rise of the characteristic $I_M = I_M\{U_M\}$ of the rectifier system in $U_M = 0$ (see Fig. 7(a) the derivation of which is explained in detail in [28].) Therefore, a symmetrical split of the output voltage can only be obtained by controlling the voltage u_M via influencing the frequency and duration of the single switching states.

Because the converter switching state is derived directly from the difference of reference and actual values of the phase currents, the possibiltiy of control interaction is basically limited to a modification of the current reference value synthesis. The only degree of freedom existing here is by addition of a zero component

$$\begin{aligned} i_{N,R}^{*\prime} &= i_{N,R}^{*} + i_0 \\ i_{N,S}^{*\prime} &= i_{N,S}^{*} + i_0 \\ i_{N,T}^{*\prime} &= i_{N,T}^{*} + i_0 \end{aligned} \tag{24}$$

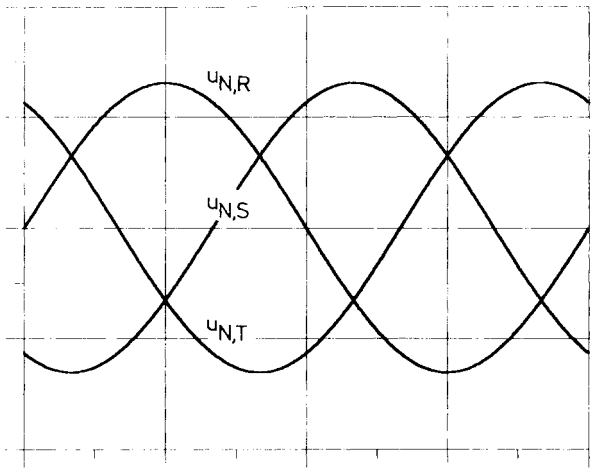
(of an offset i_0 equal for all phases) due to the amplitude $\hat{I}_N^*$ being fixed by the power to be delivered and by the sinusoidal shape required for low influence on the mains. The zero component i_0 cannot be set by the phase current controllers due to the floating mains star point $(i_{N,R} + i_{N,S} + i_{N,T} \equiv 0)$ and, therefore, does not lead to a direct influence on the mains current shape. However, it influences the frequency and duration of the switching states used for the control of the mains current and, therefore, also of the value of the center point current i_M.

According to (13) and (14), a time-constant positive value $i_0 = I_0 > 0$ in the angle interval $\varphi_U \in (-(\pi/6), +(\pi/6))$ considered leads to favoring of the switching states $s_R = 1, s_S = 0$ and $s_T = 0$, leading to a time average $I_M > 0$ (see Table I). For $I_0 < 0$ there follows in an analogous manner $I_M < 0$ [see Fig. 9(II)]. As shown in Fig. 3, with this, the quantity i_0 can be used directly for balancing of the output partial voltages.

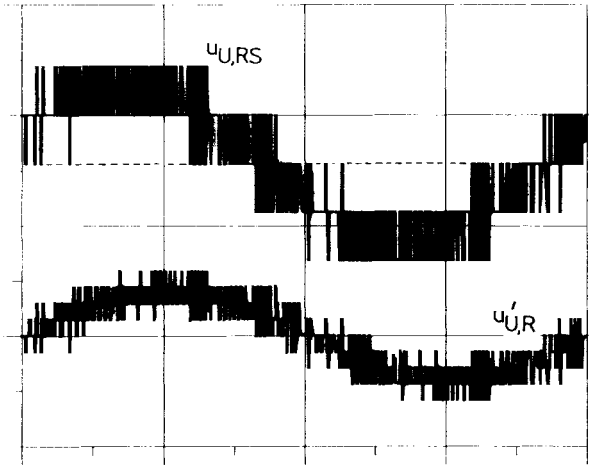
V. Digital Simulation

The results of a digital simulation of the stationary operating behavior of the system are shown in Figs. 7–9. For the purpose of a clear representation of the conditions, for Figs. 7 and 8 we chose $L = 3$ mH and/or a mean switching frequency of only $f_P \approx 3.8$ kHz. On the contrary, for a practical system realization one would have to choose a switching frequency at least above the audible spectrum, e.g., $f = 38$ kHz and/or $L \approx 0.3$ mH. The simulation results shown in Fig. 9 are based on these parameter values.

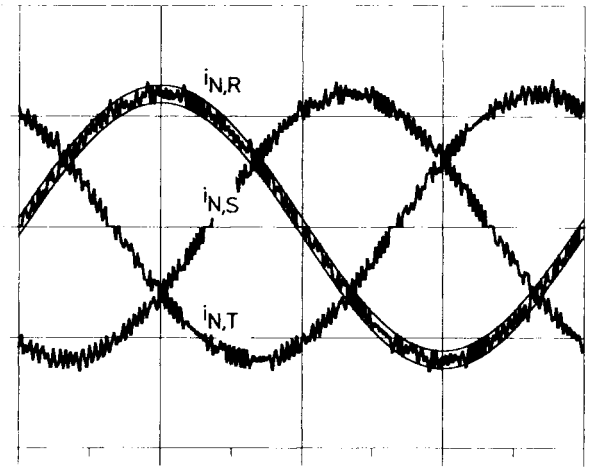
As Fig. 7(b) shows, the three-level characteristic of the bridge legs of the converter results in a very good approximation of the effective rectifier input voltage $u'_{U,i} = u_{U,i} - u_N$



(a)



(b)



(c)

Fig. 7. Digital simulation of a three-phase/switch/level unity power factor PWM rectifier. Representation for one mains period; hysteresis control of the phase currents. (a) Mains phase voltages $u_{N,(RST)}$ (related to the mains star point N, see Fig. 2), 250 V/div. (b) Line-to-line rectifier voltage $u_{U,RS} = u_{U,R} - u_{U,S}$ and phase voltage $u'_{U,R} = u_{U,R} - u_N$ determining the phase current $i_{N,R}$ in connection with $u_{N,R}$ [see (16)], 800 V/div. (c) Mains phase currents $i_{N,i}$, for phase R the switching thresholds $i^*_{N,R} + h$ and $i^*_{N,R} - h$ of the hysteresis control are shown, 15 A/div. Parameters: $U_N = 230$ V (rms), $U_O = 700$ V, $\hat{I}^*_N = 18$ A, $h = 1.5$ A, $L = 3.0$ mH.

[see (16)] to the ideal sinusoidal form. Therefore, also for relatively low average switching frequency or low rated power of the inductances L, a low rms value of the current ripple is obtained.

By the signal shapes shown in Fig. 8, the considerations concerning the control of the output center point voltage u_M via a shift by I_0 of the phase current reference values are proven. For a clear representation of the relationships, very large values I_0 are chosen (which are not characteristic for the, in reality, only low influence of the control). In general, the amount of the resulting center point current mean value I_M is determined essentially by the ratio of the amplitude of the mains currents $\hat{I}_N$ and the hysteresis width $2h$ (see Fig. 9(II) and/or [28, Fig. 12]). Due to the then high gain

$$k_M = \frac{\Delta I_M}{\Delta I_0} \tag{25}$$

of the system to be controlled, the balancing of the output partial voltages is made possible by addition of an offset I_0 being small as compared to h.

As a fast Fourier transform (FFT), which is not discussed here for the sake of brevity, of various mains fundamental periods of the rectifier input current shape shows, and as is immediately clear from a relation of the quantities

$$I_0 \approx 0.01 \cdots 0.05h \tag{26}$$

$(h \approx 0.05 \cdots 0.1\hat{I}_{N,(1),\max})$ being typical for a practical system realization, the amplitudes and the spectral distribution of the current harmonics are only little influenced there. There do not occur low-frequency distortions of the mains current. The amplitudes of the even-order harmonics (which are caused by the unsymmetry due to the shift i_0 of the phase current reference values) remain limited to the values of neighboring odd harmonics.

Fig. 9(III) shows the shape of u_M for an open and closed center point voltage control loop (where $G(s)$ is realized as a PI controller). u_M is guided along $u^*_M = 0$ (the reference value), i.e., $u_{C,1} = u_{C,2}$ until the control loop is opened in t_1. If the control loop is interrupted ($i_0 = 0$ for $t \in [t_1, t_2]$), the center point potential shows (according to the considerations in Section IV-B) a shape corresponding to the step response of an integrator with positive feedback. According to Fig. 9(I), an increasing rise of the asymmetry is connected with a reduction of the positive feedback and, finally, with a sign inversion of g_M. In the case at hand, g_M has negative values in the region $|U_M| = 50 \cdots 100$ V. Accordingly, there is inherent stability in this operating region. This can be seen in Fig. 9(III) by motion of u_M toward the zero crossing of the characterisitc $I_M = I_M\{U_M\}$ defining a value $U_M \approx 80$ V. The control loop is closed again in t_2 and, due to proper dimensioning of $G(s)$, the asymmetry of $u_{C,1}$ and $u_{C,2}$ is being corrected without overshoot.

VI. System Evaluation

For an evaluation of the proposed system, the characteristic current and voltage stresses on the devices are compared (see Table II) to those of a conventional two-level voltage dc-link PWM rectifier system shown in Fig. 10 (see e.g., Section

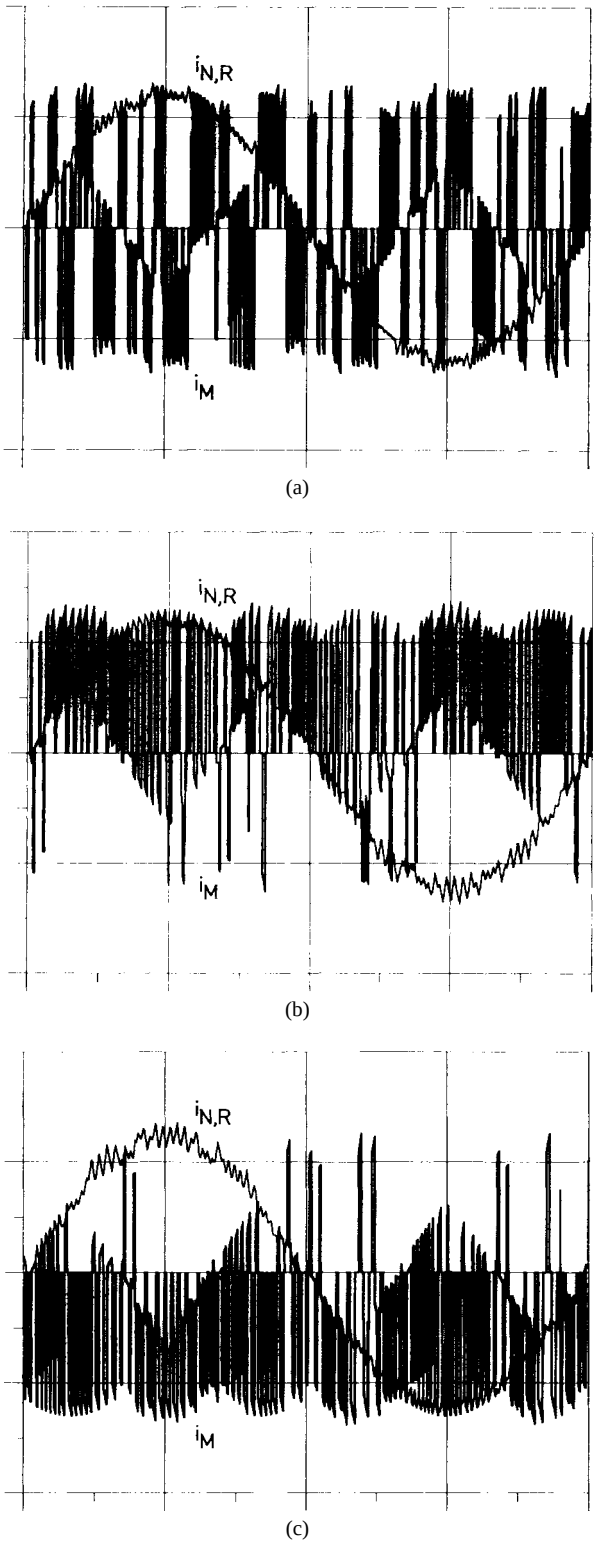


Fig. 8. Digital simulation of the function of balancing the output partial voltages $u_{C,1}$ and $u_{C,2}$ by addition of an offset I_0 to the reference values of the phase current hysteresis control (see Fig. 5). Representation of the mains phase current $i_{N,R}$ and of the current i_M loading the center point [see Fig. 2 and (20)]; 15 A/div. (a) $I_0 = 0$ (no influence of the current control), $I_M = 0.16$ A (I_M denotes the mean value of the center point current i_M within one mains period). (b) $I_0 = +0.375$ A $(+\frac{1}{4}h), I_M = +6.1$ A. (c) $I_0 = -0.375$ A $(-\frac{1}{4}h), I_M = -6.0$ A. Parameters the same as for Fig. 7.

17-7 in [29] or [30]). Because this converter circuit is also incorporated into a comparison of concepts of converters with low effects on the mains in [31] and [32], there is also given a relation to other rectifier circuits.

There has to be pointed out, however, that the circuit shown in Fig. 10 allows (contrary to the circuit described in this paper) also an energy feedback from the output circuit into the mains. One also can say that it does not have a basic limitation of the phase angle region of the mains current. Furthermore, one has to mention that the control limit is not influenced by the phase difference of the fundamentals of the rectifier input voltage and of the mains current (see Section III-C). The system operating region for resistive mains load is defined by

$$u_K \leq \sqrt{M^2 - 1}. \tag{27}$$

For given input power (and equal rating of the series inductors L), this results in a minimum value of the dc-link voltage which is lower as compared to (9). Therefore, the comparison of the component stresses as given in the following has to be seen as making reference to a (general) evaluation basis and not as a direct comparison of the circuit concepts.

The characteristic component stresses are determined by digital simulation based on nominal values:

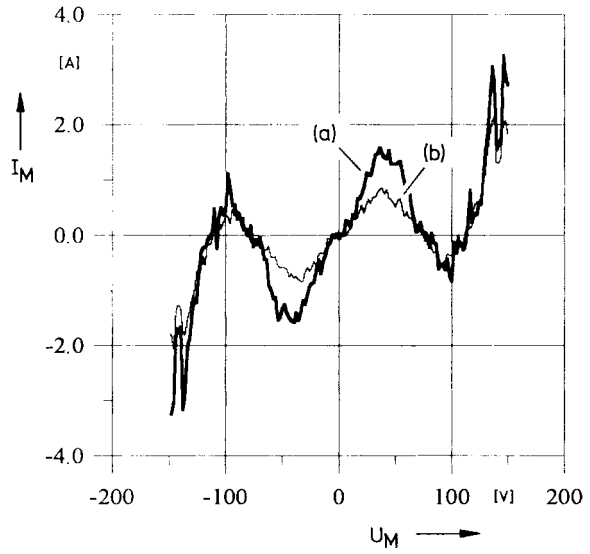
$$\begin{aligned} P_O &= 12.6 \text{ kW} \\ U_N &= 400 \text{ V}/230 \text{ V (rms)} \\ f_N &= 50 \text{ Hz} \\ U_O &= 700 \text{ V} \end{aligned} \tag{28}$$

as given for the development of a 60-V/200-A telecommunications power supply module intended to be used with the European low-voltage system. There, the control of the mains current is realized by hysteresis control, as described in Section IV-A. The phase current reference values are given proportional to the mains phase voltages [see (12)]. The efficiency of the dc/dc output stage of the module (the concept of which is laid out as an ac/dc–dc/dc converter) is estimated by $\eta_{\text{dc/dc}} = 0.95$. For the circuit parameters, we choose (as already mentioned in Section V):

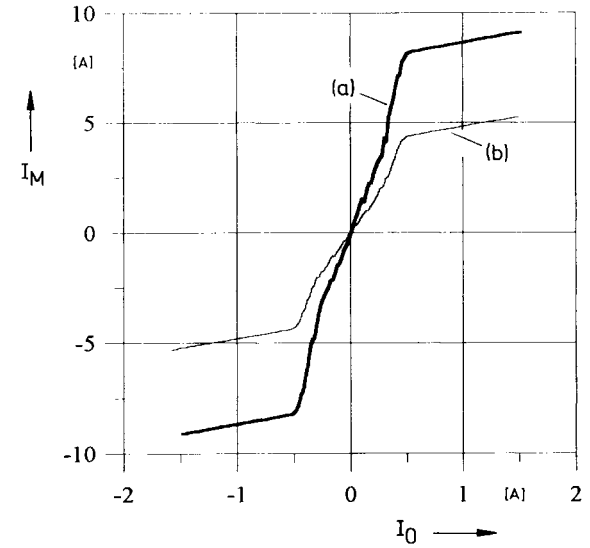
$$\begin{aligned} L &= 0.3 \text{ mH} \\ h &= 1.5 \text{ A}. \end{aligned} \tag{29}$$

As one can see from the comparison of the component stresses of the converter systems (see Table II), a significantly lower average switching frequency of the power transistors occurs for the three-phase/switch/level PWM (VIENNA) rectifier for equal hysteresis width and for approximately equal harmonic rms value $\Delta I_{N,\text{rms}}$ $(\Delta i_{N,i} = i^*_{N,i} - i_{N,i})$ of the mains current. This is obtained by the better approximation of an ideally sinusoidal shape of the rectifier input voltages due to the three-level characteristic. Therefore, for equal average switching frequency, one can reduce the value of L as compared to a realization by a two-level PWM rectifier. Furthermore, this results in a higher power/volume ratio of the converter.

A further advantage of the three-level rectifier system consists in the cutting of the blocking voltage stresses (without considering switching overvoltages) of the power transistors and freewheeling diodes, $U_{T,\text{max},i}$ and $U_{D,\text{max},i}$ into one

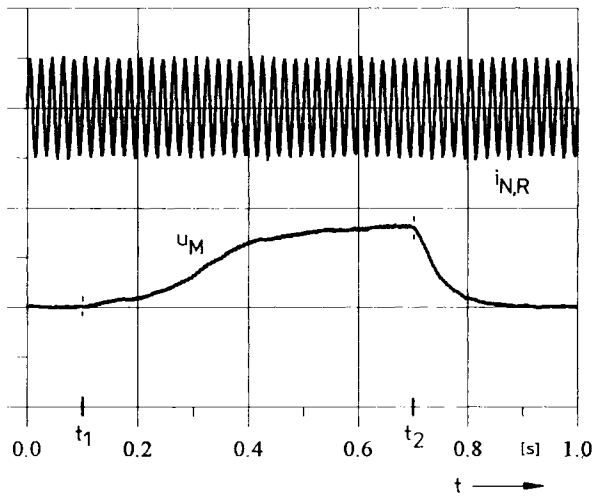


(I)



(II)

Fig. 9. For the control of the potential of the capacitive center point M of the output voltage. (I) Dependency of the mean value I_M (related to a mains period) of the center point current i_M on the (mean) center point potential shift U_M; the characterisitc can be replaced in a first approximation by a straight line $I_M \approx g_M U_M$ in the vicinity of $U_M = 0$ ($U_M = 0$ corresponds to the reference value of the controller balancing the output partial voltages). (a) $\hat{I}_N^* = 18$ A, $g_M \approx 0.04\Omega^{-1}$. (b) $\hat{I}_N^* = 9$ A, $g_M \approx 0.02\Omega^{-1}$. (II) Control characteristic $I_M = I_M\{I_0\}$ of the rectifier system; (a) $\hat{I}_N^* = 18$ A, $k_M \approx 16$; (b) $\hat{I}_N^* = 9$ A, $k_M \approx 8$. For operating parameters of the system not specified, see Fig. 7.



(III)

Fig. 9. *(Continued.)* For the control of the potential of the capacitive center point M of the output voltage. (III) Shape of u_M (100 V/div) and $i_{N,R}$ (40 A/div) for open ($t \in [t_1, t_2]$) and closed center point voltage control loop ($\hat{I}_N^* = 18$ A, capacitance of the output capacitors $C_1 = C_2 = 2.0$ mF). For operating parameters of the system not specified, see Fig. 7.

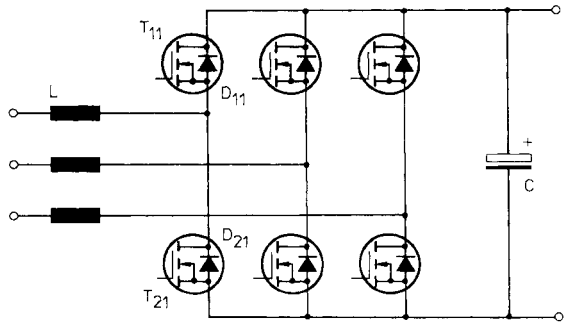


Fig. 10. Structure of the power circuit of a conventional three-phase six-switch *two-level* PWM rectifier system.

half. This allows the application of MOSFET's with lower blocking voltage and of diodes with lower reverse recovery time. With this, lower switching losses and lower transistor conduction losses (due to the lower on-resistance $R_{DS,\mathrm{on}}$ for lower blocking voltage) are obtained. This gives higher efficiency of the energy conversion.

Also, a comparison of the total volt-ampere rating $\Sigma U_{T,\max,i} I_{T,\max,i}, i = R,S,T$ ($I_{T,\max,i} = \hat{I}_{N,\max,i}$) of the transistors of the conventional system shows an advantage of the three-level converter; the two-level rectifier system requires a *four times* higher total volt-ampere rating of the power transistors.

If the two turn-off power semiconductors which are located in each of the three bridge legs of the conventional rectifier system (e.g., T_{11} and T_{21}, see Fig. 10) are paralled in each phase and used for realization of the corresponding turn-off power switch of the three-level rectifier, we have an approximately equal current stress $I_{T,\mathrm{rms}}$ for the single transistors in both cases. Also, regarding the rms values $I_{N,\mathrm{rms}}$ of the mains currents, the stresses on the diodes carrying the power flow and the stresses on the output capacitors, there are only minor differences between both systems. This checks the considerations concerning low conduction losses of the proposed system.

VII. Conclusions

Based on the basic structure of a three-phase ac/dc boost converter, in this paper, the topology of a three-phase/switch/level PWM rectifier is developed. Also, a method for controlling the output voltage and the mains current and for balancing of the partial output voltages is given.

TABLE II
COMPARISON OF THE QUANTITIES CHARACTERIZING THE COMPONENT STRESS OF A THREE-PHASE/SWITCH/LEVEL PWM RECTIFIER SYSTEM [SEE FIG. 2(b)] AND OF A CONVENTIONAL THREE-PHASE SIX-SWITCH TWO-LEVEL PWM RECTIFIER SYSTEM (SEE FIG. 10); THE STRESSES ON THE DIODES GIVEN FOR THE PROPOSED SYSTEM ARE RELATED TO THE FREEWHEELING DIODES D_{1j} AND D_{2j}; FOR THE STRESSES ON THE DIODES D_i (WHICH CAN BE REALIZED BY CONVENTIONAL RECTIFIER DIODES) OF THE BIDIRECTIONAL BIPOLAR SWITCHES WE WANT TO REFER TO FIG. 7 IN [33]; OPERATING PARAMETERS: $P_O = 12.6$ kW, $\eta_{\mathrm{ac/dc}} \approx 0.96, U_O = 700$ V, $U_N = 230$ V (rms), $L = 0.3$ mH, $h = 1.5$ A ($\approx 0.05 \hat{I}_{N,(1)}$)

Characteristic Value	Proposed System	Conventional System
$I_{N,(1),\mathrm{rms}}$ [A]	19.0	19.0
$I_{N,\mathrm{max,i}}$ [A]	29.9	29.9
$\Delta I_{N,\mathrm{rms}}$ [A]	0.62	0.65
$I_{T,\mathrm{avg}}$ [A]	5.1	1.3
$I_{T,\mathrm{rms}}$ [A]	8.6	4.5
$U_{T,\mathrm{max,i}}$ [V]	350	700
$I_{D,\mathrm{avg}}$ [A]	6.0	7.3
$I_{D,\mathrm{rms}}$ [A]	11.5	12.4
$U_{D,\mathrm{max,i}}$ [V]	350	700
$I_{C,\mathrm{rms}}$ [A]	9.3	9.5
$f_{P,\mathrm{avg}}$ [kHz]	33.3	57.3

In the following, the advantages and disadvantages being relevant for a qualitative evaluation of the converter concept (as can be used, e.g., for a concept study) are summarized briefly.

Advantages are the following:

- simple structure of power and control circuit, only one power transistor per phase (low control/driving effort);
- possibility of realization of the control circuit by analog techniques—high dynamics, avoidance of the development effort associated with the application of microprocessor control;
- low harmonics rms value of the mains current due to inclusion of the center point of the output voltage into the synthesis of the rectifier input phase voltages (three-level characteristic); for hysteresis control of the input currents: distribution of the power harmonics over a wide frequency range due to time-varying switching frequency [34]—as compared to constant switching frequency a lower filtering effort for compliance to the regulations concerning conducted EMI [35] is required;
- low blocking voltage stress on the power semiconductors (possibility of application of low-voltage MOSFET's and ultrafast recovery diodes even for high dc-link voltage, e.g., for an output voltage of $U_O = 700$ V valves with a blocking voltage capability $\mathrm{V_{DSS}} = \mathrm{V_{RRM}} = 500 \cdots 600$ V can be applied—low transistor conduction losses and low switching losses (the blocking behavior of the diodes has an essential influence on the resulting switching losses [36]); *remark:* the diodes D_i of the bidirectional bipolar switching elements [see Fig. 2(b)] are not commutated with switching frequency and, therefore, can be realized by conventional rectifier diodes;
- low nominal power of the inductances connected in series on the mains side (high dynamics of the dc-link voltage control and/or reduction of the dc-link capacitance required for buffering of load steps)—high power/volume and/or power/weight ratio of the converter;
- as compared to bridge circuits: 1) significantly higher utilization of the power transistors (conduction of each transistor during positive *and* negative half period of the related phase current); 2) for realization of the power transistors by power MOSFET's no current flow occurs through the parasitic internal diodes of the devices and/or a possible conduction of these diodes doesn't have to be suppressed by diodes lying in series with the power transistors (see [37, Fig. 1]); 3) higher reliability of operation—in the case of a control malfunction of a power transistor, no short circuit of the output voltage occurs; and 4) lower common-mode EMI (lower EMI filter requirement);
- possibiliy of distributing the load to the positive and negative output partial voltages; there, $u_{C,1}$ and $u_{C,2}$ can be loaded very much unsymmetrically because, for appropriate system control, one obtains a high current handling capability of the output voltage center point M [38];
- possibility of operating the system with inductive mains phase current angle allows a partial compensation of the capacitive reactive power caused by an EMI filter; furthermore, this gives a degree of freedom for an optimization of the mains filter (see [39, Figs. 7, 8]).

Disadvantages are the following:

- limitation of the system operating region concerning the phase angle of the mains current and voltage transformation ratio M (see Section III-C), especially limitation to unidirectional energy conversion;
- relatively high circuit effort for the realization of the converter by discrete devices; this can be avoided by application of a power module which integrates a bridge leg of the system (e.g., the module IXYS VUM25-E has been designed for $U_N = 230$ V and $U_O = 700$ V and permits the realization of a rectifier system with $P_O = 15$ kW, $f_P = 50$ kHz und $\eta_{\mathrm{ac/dc}} = 0.96$ [33]);
- for hysteresis control of the input currents by independent phase controllers: current control error possible in the order of magnitude of twice the hysteresis width; occurrance of limit cycles [27]—nonoptimal utilization of the converter pulse frequency.

In order to minimize the effort regarding the circuit technology and/or of development, system and fabrication costs in the present case a simple control method (i.e., hysteresis control of the mains currents, which can be realized by analog means) has been selected. Naturally, this does not lead to a minimization of the harmonics rms value of the mains current or of the switching frequency. The possibility of a relevant optimization (described in the literature for three-level PWM *inverters* [40]–[42]) is only given when the converter control

unit is realized by digital means, e.g., when a signal processor system is used. This is presently the topic of further research.

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Johann W. Kolar (M'89), for a photograph and biography, see p. 123 of the February 1997 issue of this TRANSACTIONS.

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DESIGN OF SINGLE PHASE BOOST POWER FACTOR CORRECTION CIRCUIT AND CONTROLLER APPLIED IN ELECTRIC VEHICLE CHARGING SYSTEM

by

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ABSTRACT

In this thesis, based on the existing researches on power factor correction technology, I analyze, design and study the Boost type power factor correction technology, which is applied in the in-board two-stage battery charger.

First I analyzed the basic working principle of the active power factor corrector. By comparing several different topologies of PFC converter main circuit and control methods, I specified the research object to be the average current control (ACM) boost power factor corrector.

Then I calculated and designed the PFC circuit and the ACM controller applied in the first level charging of EVs. And I run the design in Simulink and study the important features like power factor, the input current waveform and the output DC voltage and the THD and odd harmonic magnitude.

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Chapter 1: Introduction

1.1 Project Background

With the high modernization and electrification of industry, people now have a higher requirement for the power quality. For instance, personal computers, electronic devices, cell phones, they each has a basic requirement for power quality. Bad power quality may cause the electronic devices not working properly or even not working. For power quality, power factor is a significant factor, which impacts power quality directly. Small power factor will cause many negative effects, such as power grid waveform distortion and large line loss, which may reduce the service time of power devices.

As electricity gets more and more important in people's life, there are increasing number of power devices with different features. The power we get from national grid is 110V and 60 Hz. But most of the power devices require a different input from what we get from national grid, so we have to make some conversion of the voltage and current. There are 4 kinds of conversion circuits as below: AC-DC circuit, DC-DC circuit, DC-AC circuit and AC-AC circuit. AC-DC conversion circuit, which converts current to direct current, is most used in industry nowadays. And we call this kind of circuit rectifier circuit. Rectifier circuit has many applications, such as appliances like uninterrupted power supply(UPS). Rectifier circuit can act as interface circuit between power grid and power electronic devices, composing DC regulated power supply, and supplying high quality power for power electronic devices.

Power factor is a significant qualification of power system. With the wide application of power electronic in industry, switching devices are widely used in different power conversion devices. The introducing of switching devices improved the devices' efficiency of power conversion but brought problems like harmonic pollution and low power factor. In order to eliminate harmonic and improve power factor, people bring a new technology which is called power factor correction. Because people now are trying to get high quality power, power factor correction is in leading edge of power electronics research.

Power factor correction is very important because low power factor brings lots of problems to our circuits and power devices. The key point to improve the power factor of power devices is the research of topology structure of power factor correction circuit and integrated circuit of power factor correction. There are several popular chips used to achieve power factor correction, like L4981, UC3842-UC3855A series, KA7534 and TDA4814. [1]

Boost circuit is a basic DC-DC conversion circuit. Boost circuit has many advantages like continuous inductor current, less distortion of current waveform and less RFI and EMI noise, so boost circuit is widely used in different power design. But for basic boost circuit, there are some perspectives we can improve such as power factor and circuit transmission efficiency.

Because of the wide application of power electronic devices, there are reactive power and harmonics in the power grid. One of the method to solve this problem is to apply active power factor correction technique. This technique brings active switch into

conversion circuit, through the control of on and off of active switch, we can make input current follow the input voltage. So we can make a sinusoids shape input current and a power factor which approaches 1. The main research content of this paper is the design of boost power factor correction circuit and design of its control system.

1.2 Disadvantage due to Harmonic Current in Power Grid [2]

In fact, the decrease of power factor caused by harmonic current already exists for a long time. People don't pay much attention because the use of switching devices is not widely used and people know little about the disadvantage of harmonic current. Generally speaking, there are always harmonics wherever there are switching devices. The existence of harmonics will lead to decrease of power factor. In earlier years, people use thermistor and rectifier diodes a lot, so there are problems like harmonic current and low power factor in power electronic devices.

Impulse shaped AC input current waveform contains a lot of harmonic current components. These Harmonic current components will pollute power grid. Harmonics in an electric power system are a result of non-linear electric loads. It will produce current in a different frequency from its original frequency. Harmonic current has following disadvantages:

(1) The 'secondary effect' of harmonic current, which is, when harmonic current passes the loads, it will cause harmonic voltage which will distort the voltage of power grid, so there will be overcurrent or overvoltage.

(2) It will increase the extra loss of the circuit, and decrease the efficiency of the power

generation equipment and power transmission equipment.

(3) It will make power devices (such as transformer, capacitor and electric motor) work abnormally, accelerate the insulation aging and abbreviate the devices' service life.

(4) It will make relay protection, automatic devices and computer system work abnormally or even don't work.

(5) It will make measuring equipment or instrumentation not able to measure.

(6) It will interfere communication systems, decrease the transmission quality of signal, or even damage the communication devices.

So we can conclude that the existence of harmonic current pollute power grid so much and we have to take some actions to eliminate or restrain harmonic current. There are two ways to restrain harmonic current, the first is to use reactive power compensation device to produce harmonic which has the same frequency but opposite phase. The second way is to produce some devices which doesn't produce harmonic current.

1.3 PFC in EV Front-End AC-DC Converter Applied in Charger

In the EV charging system, the front-end AC-DC converter is very important and should meet the requirements of the efficiency and power density. And this thesis focuses on the AC/DC PFC boost converter component and the its controller. The system block diagram of a universal in-board two-stage battery charger in Fig.1.1 [3] [4].

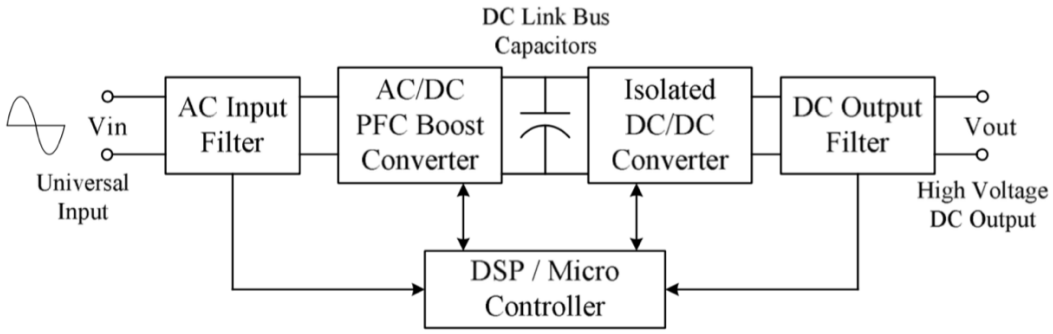


Fig.1.1 Simplified system block diagram of a universal in-board two-stage battery charger

1.4 The Main Content of the Research

a. Learn the control strategy of power factor correct circuit.

b. Learn the principle and basic control strategy of boost converter power factor correction circuit.

c. Simulate the boost converter power factor correction circuit applied in EV level 1 charger.

Chapter 2: Single Phase APFC's Main Power Topology and Its Control Strategy

The main contents of this chapter are as follows:

(1) Activate power factor correction.

(2) The main power topology structure of APFC and its modified topology structures.

(3) The typical control strategy of APFC.

(4) The advantages and disadvantages of Boost APFC.

The basic idea of PFC is using power conversion of high frequency switching mode to make the shape of input current close to sinusoidal wave. One of the popular ways is to have a value which is in proportion to the input voltage to be the reference of the current. For this way, we just assume that the harmonic of the input voltage is small and can't effect the control of harmonic current. In most cases, the correction of power factor is achieved by an an independent part which is called PFC (power factor corrector). The input of the PFC is usually power grid, and the output is usually a DC voltage. The DC voltage will be the input of DC-DC converter or DC-AC current and provides a stable output for the next converter, making the DC-DC converter or DC-AC converter becomes an optimal design.

2.1 Active Power Factor Correction(APFC)

2.1.1 The definition of AC-DC converter power factor and its relationship with harmonic waves [4]

In linear circuit, we use cosφ to express power factor, of which φ is the phase difference of sinusoidal voltage and sinusoidal current. Because diodes in the rectifier circuit is not linear, although the input voltage is sinusoidal, the rectified current is non-sinusoidal. So the power factor calculation in linear circuit is no longer valid in AC-DC converter. We use PF to express power factor here.

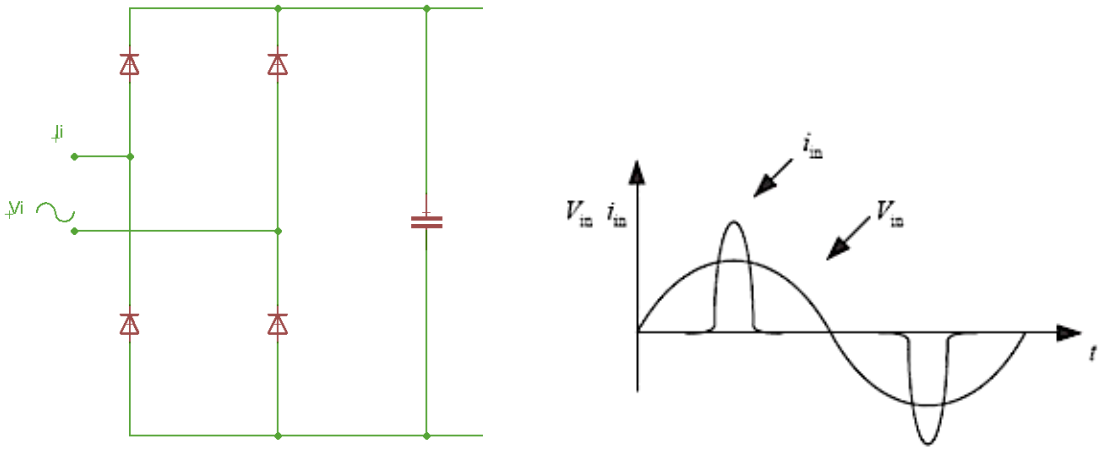


Fig.2.1 Rectifier circuit and its input voltage and current waveform

The definition is PF=active power/apparent power=P/V•I.

In the equation above, V and I here are the rms voltage and rms current.

We assume the input voltage v_i (rms value is V) is sinusoidal, and input current is not sinusoidal, the rms of current is shown as follow:

$$I = \sqrt{I_1^2 + I_2^2 + \cdots + I_n^2 + \cdots} \tag{2.1}$$

In this equation, I_1, I_2, ..., I_n are respectively the fundamental component, second harmonic, …, and N^{th} harmonic.

Because the input current has a terrible distortion and phase change, the definition of the power factor used in linear systems is not available anymore in switching power systems. We assume that i_1 lags v_i by phase α, as shown the figure below:

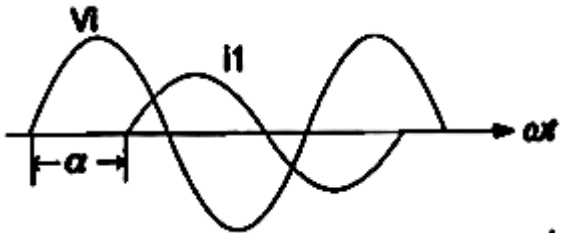


Fig.2.2 The V_i, i_l waveform

$$P = VI_1 \cos\alpha \tag{2.2}$$

$$PF = VI_1 \cos\alpha / VI = I_1 \cos\alpha / I \tag{2.3}$$

And we know that,

$$I_1/I = I_1/\sqrt{I_1^2 + I_2^2 + \cdots + I_n^2 + \cdots} \tag{2.4}$$

I_1, I_2, ..., I_n are rms value of the fundamental component, second harmonic, …, and N^{th} harmonic. The equation above describes the relative magnitude of the fundamental current, which is called distortion factor. And cosα is called displacement factor, and the power factor equals the distortion factor times the displacement factor. When α=0, PF=I_1/I.

We call the total harmonic distortion THD, so

$$THD = I_h/I_1 = \sqrt{(I_2^2 + I_3^2 + \cdots + I_n^2 + \cdots)/I_1^2} \tag{2.5}$$

I_h is the rms value of all the harmonic currents.

So we can get the equation of distortion factor:

$$I_1/I = 1/\sqrt{1 + THD^2} \tag{2.6}$$

And when α=0,

$$PF = I_1/I = 1/\sqrt{1 + THD^2} \tag{2.7}$$

2.1.2 Basic principle of APFC [5]

The circuit of APFC contains two parts, one is the main circuit and the other is the control circuit. We take boost PFC circuit as an example. From Fig.2.3 [6] we can see, the main circuit consists of a single-phase bridge rectifier and DC-DC converter. And for control circuit, we have reference voltage ($V_{o,\,ref}$), voltage error amplifier (VA), multiplier (M), current error amplifier (CA) and pulse width modulator (PWM).

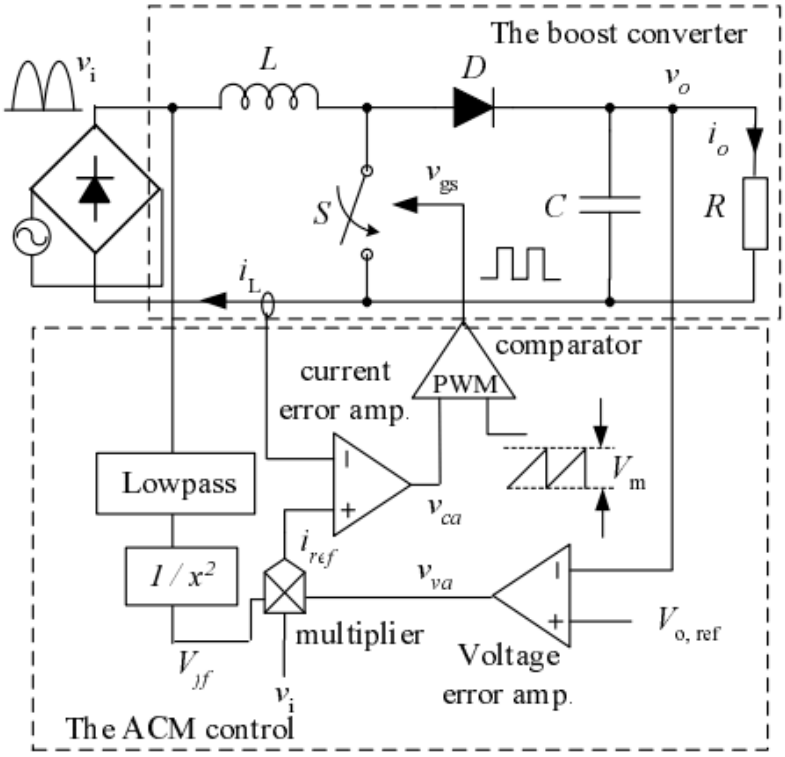


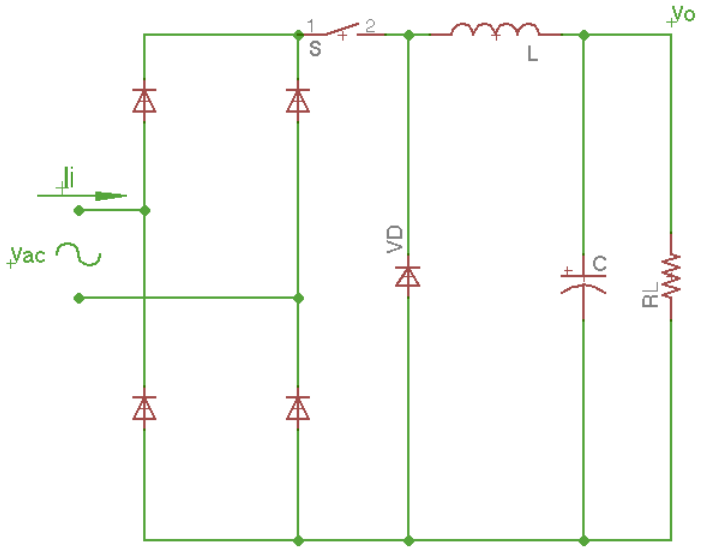
Fig.2.3 Simple schematic of the boost APFC under ACM control

Now we discuss the principle of PFC. After comparing the output voltage with the reference voltage, the result goes through the voltage error amplifier. The output of voltage error amplifier and rectified input voltage together go to multiplier and we set the output of the multiplier as the reference of current feedback control. After comparing the reference current with the input detected current, the result goes into the current error amplifier and control the on and off of the switch S. So we can make the input current and the rectifier input voltage be at almost the same phase, and there is less harmonic current, that we can increase the power factor and make the output voltage stable.

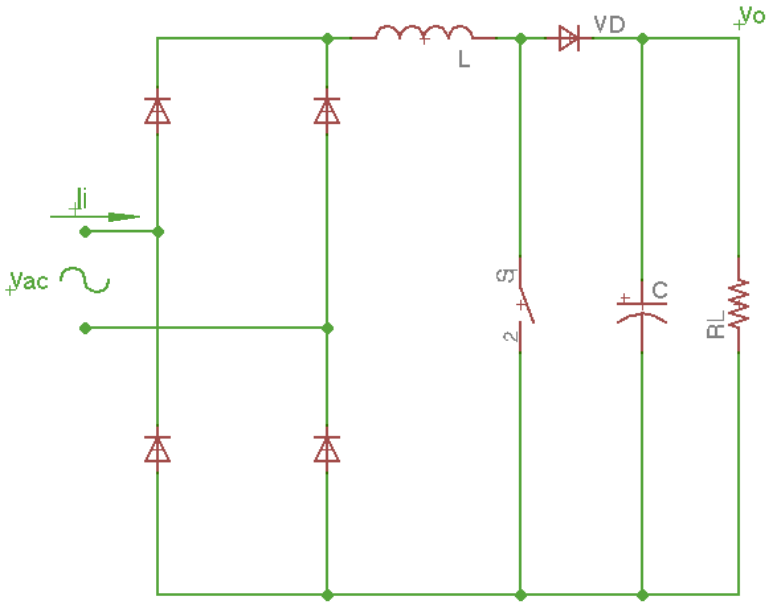
2.2 The Topology Structure of APFC

2.2.1 Several typical topologies of APFC

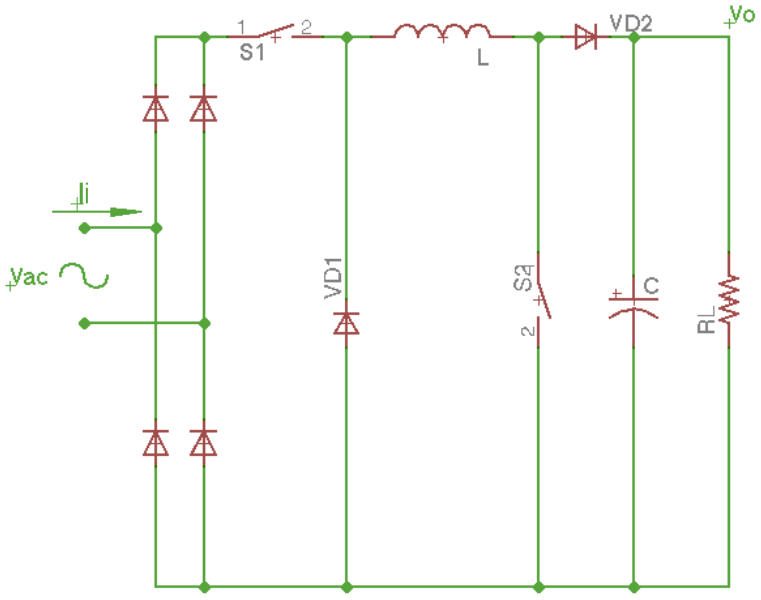
There are many kinds of topologies of APFC, the typical topologies of APFC are Boost, Buck, Boost-Buck, Ćuk and flyback converters. Boost converter is most used because it has several advantages against other APFC circuits. Boost and Buck converters have the most basic topology structures among all APFC circuits and other structures are developed from these two structures. Now we simply talk about the features of Boost, Buck, Boost-Buck and Ćuk converters.



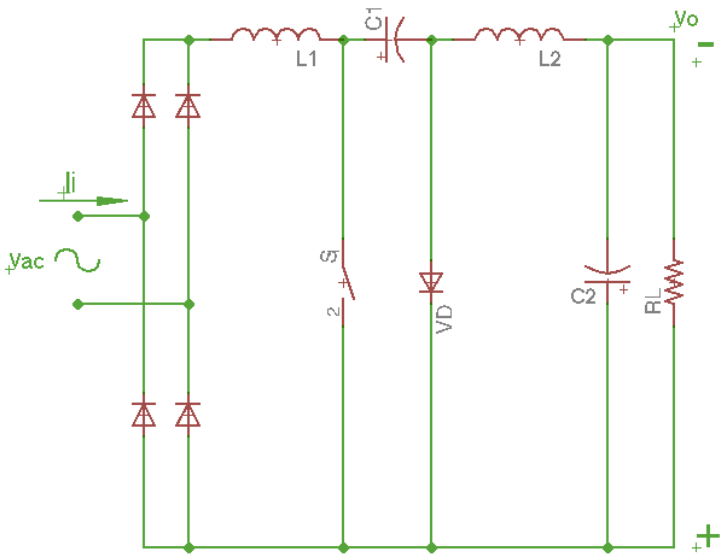
(a) Buck PFC



(b) Boost PFC



(c) Buck-boost PFC



(d) Ćuk PFC

Fig.2.4 Several topology structure of PFC

a. Buck converter:

(1) Buck converter can only buck the voltage because when the switch is on, the inductor L and conductor C are in series connection.

(2) The input current of the source is discontinuous because when the switch S is off, V_{ac} and inductor L, conductor C are insulated. So it restricts the efficiency of the converter and leads to high ripples of the input current.

(3) When switch is on, the source voltage is V_d. But when switch is off, the source voltage is 0. So when the input voltage is high, we need a specific floating drive for the switch since the source voltage is float. As a result, it makes the design of circuit more complicated.

(4) Because buck the converter can only be used to buck voltage, we cannot use it for APFC

directly, because the source voltage V_d is a half sinusoidal waveform after rectified by the full bridge rectify. So for 110VAC source, the variation range of V_d is from 0 to 155.56V. And when V_d is smaller than the output voltage Vo, the converter can't work, which restricts the increase of the power factor.

b. Boost converter:

(1) When boost converter is the main circuit of PFC, it can only boost the voltage so that this circuit is working stably. The inductor L is charged when switch S is on and when switch S is off, L is discharged.

(2) The AC input current is always the same with inductor current, so that input current is continuous. When implementing large power DC-DC converting and power factor correction, the continuous input current has its own advantage. At the same time, the ripple current is small when input current is continuous, so it reduces the processing requirements for the filter circuit.

(3) Because the source voltage of the switch is always 0, it's easy to control the switch.

c. Buck-Boost converter:

(1) When we take Buck-Boost converter as the main PFC circuit, we can either buck voltage or boost the voltage, which can get over some disadvantages of the circumstances that we have only boost converter or buck converter.

(2) The input current of the source is discontinuous, which is the same with the Buck converter because the input itself is a Buck converter. So it increased the requirements for the filter circuit.

(3) When we use Buck-Boost converter as the main PFC circuit, we need two switches

(one for drive control). so the circuit is more complicated.

d. Ćuk converter:

The main idea of Ćuk converter is to have a series connection of a Boost converter and a Buck converter.

(1) Whether the switch S is on or off, the current of inductor L1 and L2 is continuous, and the input source current is always the same with the current in the inductor L1. And this feature is the same with the Boost converter.

(2) When we increase the inductor L1 and L2, we can make ripple current very small. So we don't need extra EMI filter, and the devices can be miniaturized.

(3) Ćuk converter can either buck or boost the voltage like Buck-Boost converter.

2.2.2 Several topologies of modified single phase PFC

a. Center tapped boost inductor circuit

The center tapped boost inductor circuit is like the figure below. Through adding several coils on the magnetic ring of the boost inductor, the drain of the MOSFET is not connected to the boost diode directly. And we know that the inductor current cannot be mutated so that we can restrain the large instantaneous current caused by backward recovery of the boost diode D1. And we can restrain the overheat caused by the large opening loss. The main disadvantage of this circuit is the ripple noise of output voltage caused by the backward recovery of D1. So we have to add a LC filter at the output to eliminate the ripple.

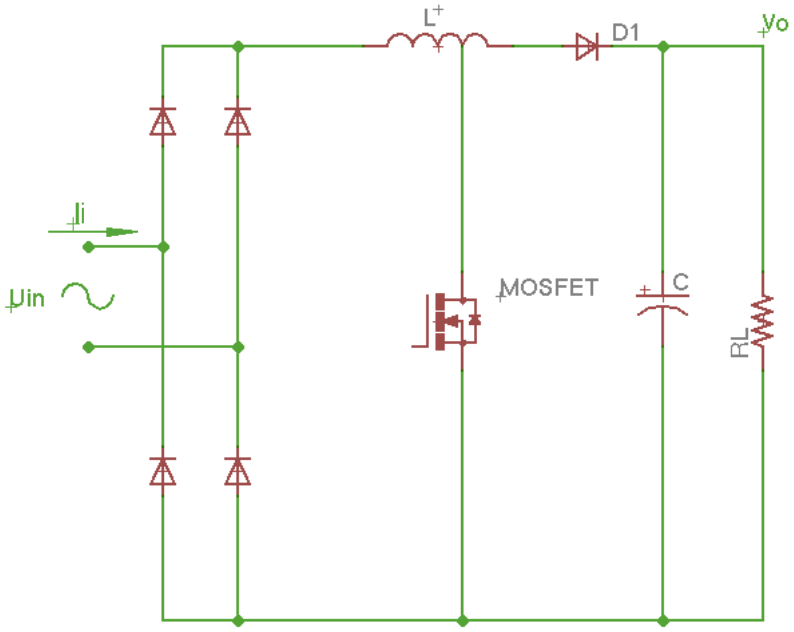


Fig.2.5 Center tapped boost inductor circuit

b. Series inductor and RCD snubber circuit and clamp circuit

As shown in Fig.2.6 and Fig.2.7, through increasing L2 we can restrain the impulse current caused by the backward recovery of D1. But when the MOSFET is cut off, we have to solve the problem of overvoltage generated by L2 on the switch.

In the upper figure, we use D2, C2 and R1 to compose RCD snubber circuit. Because capacitor voltage cannot be mutated, and we can use that to restrain the overvoltage caused on L2 by cutting off of the MOSFET. The overvoltage on the capacitor is released to the 400V output, so we can protect the switch from the overvoltage.

In the lower figure, R1, C1 and D2 composed clamp circuit. Because in PFC circuit, we tend to use a large electrolytic capacitor filter at the output, we can hold up the output

voltage at 400V. So we can use the clamp characteristics to restrain the switch voltage in the rated voltage range across the transistor switch.

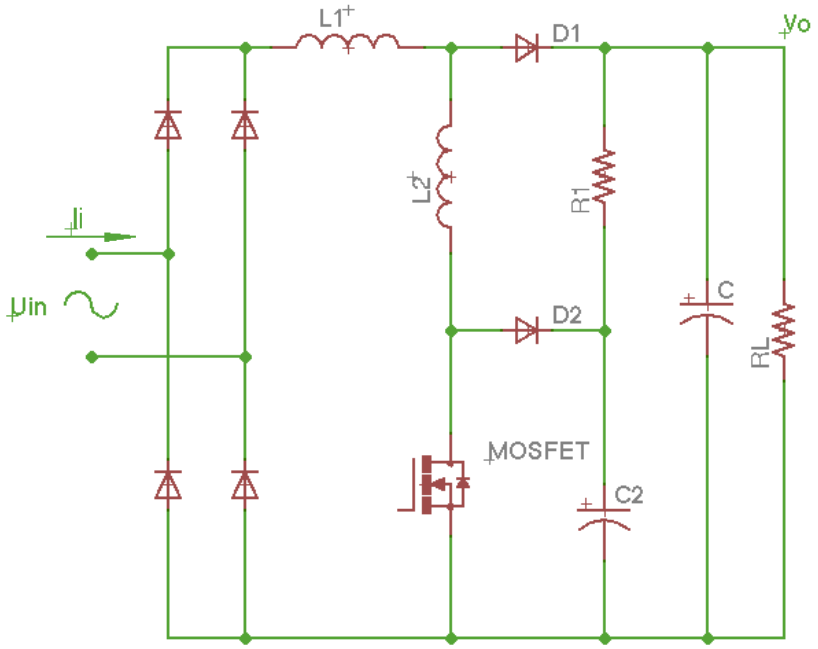


Fig.2.6 Series inductor and RCD snubber circuit

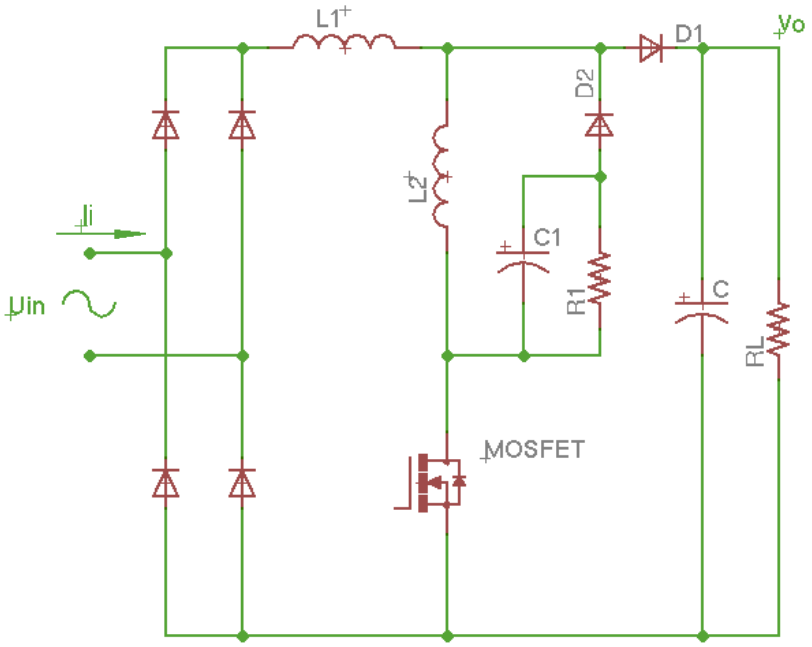


Fig.2.7 Series inductor and clamp circuit

c. Series inductor and lossless snubber circuit

In this circuit, we add C1 and D3 to be the snubber circuit of diode D1. When the switch is off, the current flow through L2 and charge the snubber capacitor C2 and the junction capacitance of switch. Because we added snubber capacitor, the rising speed of the voltage will be slowed, so that we achieve the shutdown buffer. In addition, the series connection of D2, D and D3 can restrain the impulse current of the switch.

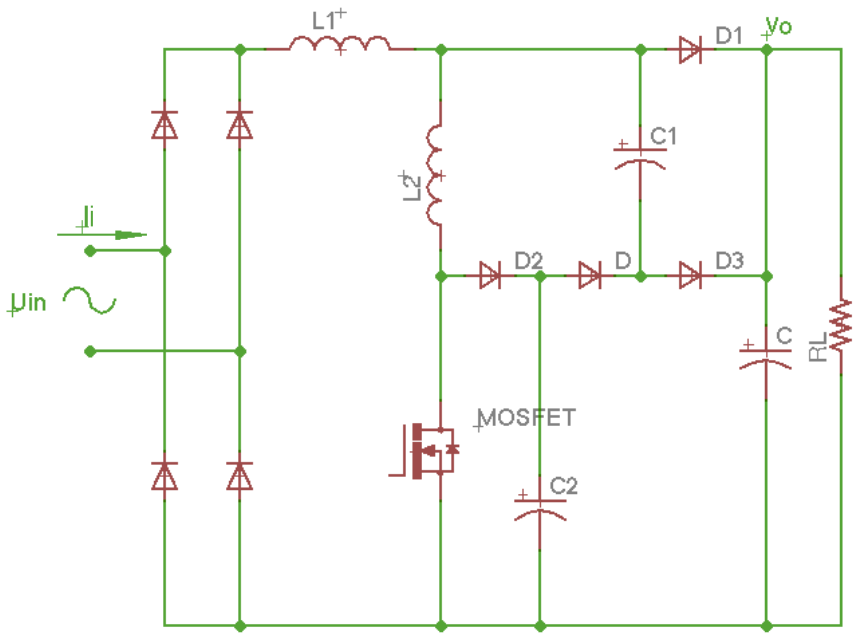


Fig.2.8 Series inductor and no loss snubber circuit

d. Series Schottky diodes circuit

In Fig.2.9, D1, D2 and D3 are all Schottky diodes. Since the backward recovery time of Schottky diode is very small (less than 10ns), we can use Schottky diode to restrain the impulse current. Schottky diode has small withstand voltage, so we just apply series structures of D1, D2 and D3. This series connection will also decrease the impulse current of the switch. But this circuit has high requirements for the withstand voltage and the consistency of the dynamic and static characteristics of Schottky diode.

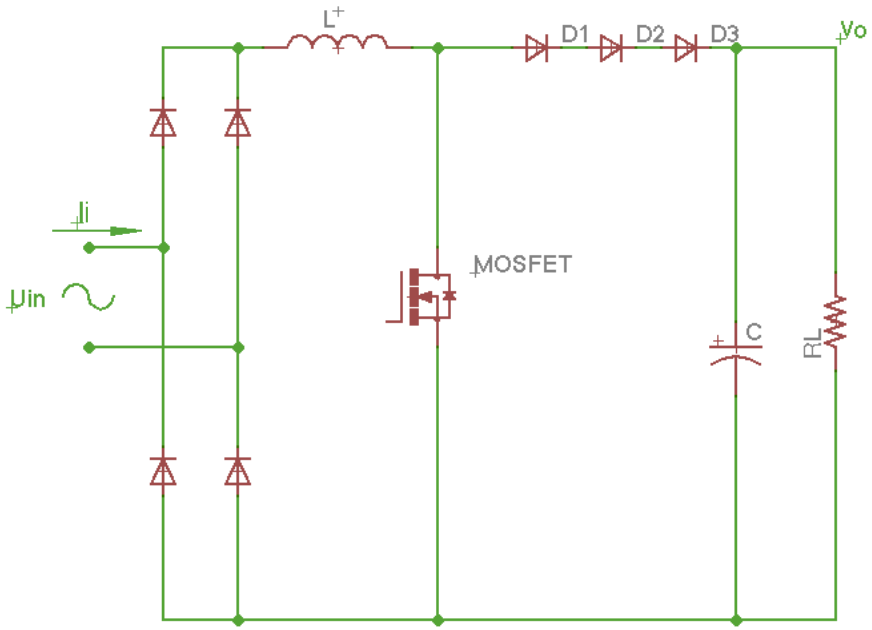


Fig.2.9 Series Schottky diode circuit

2.3 Typical Control Strategy of APFC

In practical applications, we have different control strategies for different APFC topologies. No matter what APFC topology we use, in order to achieve PFC, we have to take control of two variables:

a. Output voltage, that we have to make sure is stable DC voltage.

b. Input current, that we have to make to follow the input voltage at the same frequency and the same phase, and make the input port to be pure resistance.

Therefore, for APFC, we usually apply Voltage-Current double-loop feedback control strategy. In some cases, it will make the PFC circuit more complicated. Because Boost converter has many advantages, like it is easy to control, and it has continuous input

current and small ripple current, it is widely used in industry. So we take Boost converter as an example to analyze the control strategy.

There are two goals we need to achieve for APFC strategy, which are stabling the output voltage and realizing unit input power factor. And there are many different control schemes presented by many scholars to fulfill the different requirements in different circumstance. We can divide APFC into two types according to whether the inductance current is continuous. One is DCM (Discontinuous Conduction Mode) and the other is CCM (Continuous Conduction Mode) [7] [8]. In CCM, we can achieve PFC using multiplier. While in DCM, we realize PFC using voltage follower. Under CCM, the control strategy is furtherly divided into two methods according to whether we use the instantaneous inductor current as feedback. Direct current control adds the current feedback. And for Indirect current control, current feedback is not added.

2.3.1 Discontinuous conduction mode

We call Discontinuous Conduction Mode as Voltage-follower Control. There are two control modes, one is constant frequency mode and the other is variable frequency mode [9]. In order to get steady output voltage, we need output voltage closed loop feedback control, of which the switch is controlled by the output voltage error signal. During one switching circle, the mean value of the inductor current is in proportion to the output voltage, so that the input current follows the input voltage automatically.

a. Constant frequency mode

Fig.2.10 shows the DCM control strategy of Boost circuit. We set the frequency bandwidth of voltage regulator at 10-20Hz, so that the duty circle is steady during half of the frequency period. In constant frequency mode, the switching frequency stays constant and the inductor current is discontinuous. And the average inductor current during a switching cycle is written as below [10]:

$$I_{avg} = \frac{V_d T_{on}(T_{on}+T_{don})}{2LT_s} \tag{2.8}$$

V_d is the rectified voltage, Ton is the conducting time when the switch S is on, T_{don} is the freewheeling time of the diode VD and T_s is the switching cycle.

In the equation, we assume T_{don} is constant and we take the input port of DC-DC converter as pure resistance. So for the AC side, the voltage and the current are of the same phase. Actually, T_{don} is not constant so there is some degree of distortion of the average input current. The greater the ratio of the output voltage over the peak of the input voltage, the smaller the distortion will be [11].

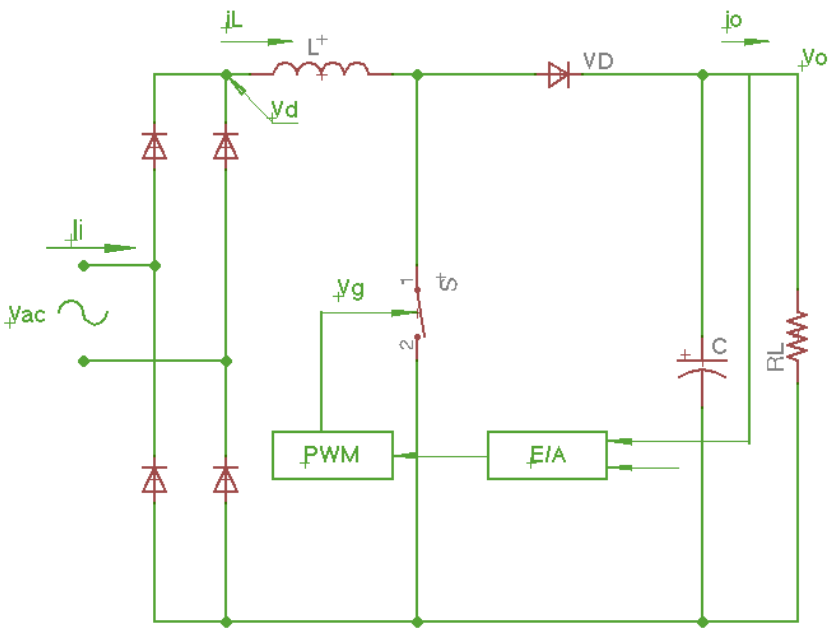


Fig.2.10 DCM mode of boost circuit

b. Variable frequency mode

In the equation (2.7), if $T_s=T_{on}+T_{don}$, the average input current is only related to the time when the switch is on. So if T_{on} is constant, there should be no distortion on input current, and this is how the variable frequency mode works. When the duty circle and the switching frequency is constant, the average input current is in proportion to the input voltage. So we don't have to regulate the current, and the average input current is following input voltage automatically.

- Advantages of DCM mode:

(1) The circuit structure is simple, and it is not necessary to add multiplier.

(2) The input current follows the input voltage automatically.

(3) The diode won't suffer the impulse current caused by backward recovery.

- Disadvantages of DCM mode:

(1) The inductor current is discontinuous so there is large ripple current, and the filter need to satisfy high requirements [12].

(2) The output contains the second harmonic, and the power devices take a little bit large current stress.

(3) The power of the single phase PFC is usually smaller than 200W.

2.3.2 Continuous conduction mode (CCM)

We can divide CCM into two control mode, one is indirect current control, and the other is direct current control.

a. Indirect current control mode

For indirect current control, it's also known as phase amplitude control. It is a control mode which is based on steady frequency. Through regulating the input voltage of the rectifier, making it at specific phase and amplitude related with source voltage, we can regulate the AC input current to be sinusoidal wave, and also at the same phase with the input voltage. The advantage of this control mode is that its structure is clean and easy to build [13]. And there are also some disadvantages of this circuit. It can't limit the current, so we have to add an overcurrent protection circuit. Furthermore, in transition from a steady state to another, there will be DC component in current wave. In addition, the dynamic response of this system is slow.

b. Direct current control mode [4] [14]

In direct current control mode, the circuit contains multipliers so it is also called multiplier approach control. The basic idea of this control mode is to feed the input voltage signal and the output voltage signal into the multiplier, and then make the output signal of multiplier as reference current signal of current controller. The current controller will control the input current to vary and follow the reference signal. The disadvantage of this circuit is that the circuit is kind of complicated compared to indirect current control. In this control mode, we sometimes need to add a current loop compensation network; the output contains second harmonic; the dynamic response is also very slow; and the nonlinear distortion of multiplier will increase the harmonic in the current. Because the input current always contains ripple of switching frequency, we have to decide which current should be the feedback. So there are three kind of control mode. The first one is peak current mode control. The second one is hysteresis current mode control and the last one is average current mode control. These three control modes are widely used in APFC.

Now we take Boost PFC circuit as an example to introduce the principle of these three control modes. And we assume they all work as CCM.

(1) Peak current mode control

Fig.2.11(a)-(b) shows the schematic diagram of peak current mode control. The switching period is T and stays constant. We multiply the input voltage signal with the feedback signal of the output voltage, and we can get a current control reference signal which is the same phase and same frequency with input voltage. When the switch is on and inductor L is getting charged, we compare the inductor current with the current

control reference signal. When the inductor current rises to the reference signal, the switch is shut down by logical control. Then the inductor starts discharging, and after a switching cycle the switch is closed again. Fig.2.11(b) shows the inductor current i_L and switch control voltage V_g.

As the peak of inductor current increased sinusoidal, the duty circle of control waveform will vary from a large value to a small one. During half of the switching cycle, the duty cycle is sometimes greater than 0.5 and sometimes smaller than 0.5. When the duty cycle is larger than 0.5, the outside interference will be amplified, and the system current is not convergent, which may lead to sub-harmonic oscillation. So it is necessary to add a slope compensation or a ramp. Under this condition, the circuit will work well and stable when the duty circle changes [4] [11].

The main problem of Peak Current Mode Control is that we are trying to control the peak of inductor current, but we cannot ensure that average input current is in proportion to input current. And in some cases, it will generate a large error, so there might be large distortion which we don't expect. On the other hand, the peak current is very sensitive to noise. So in PFC circuit, we don't tend to use peak current mode control anymore.

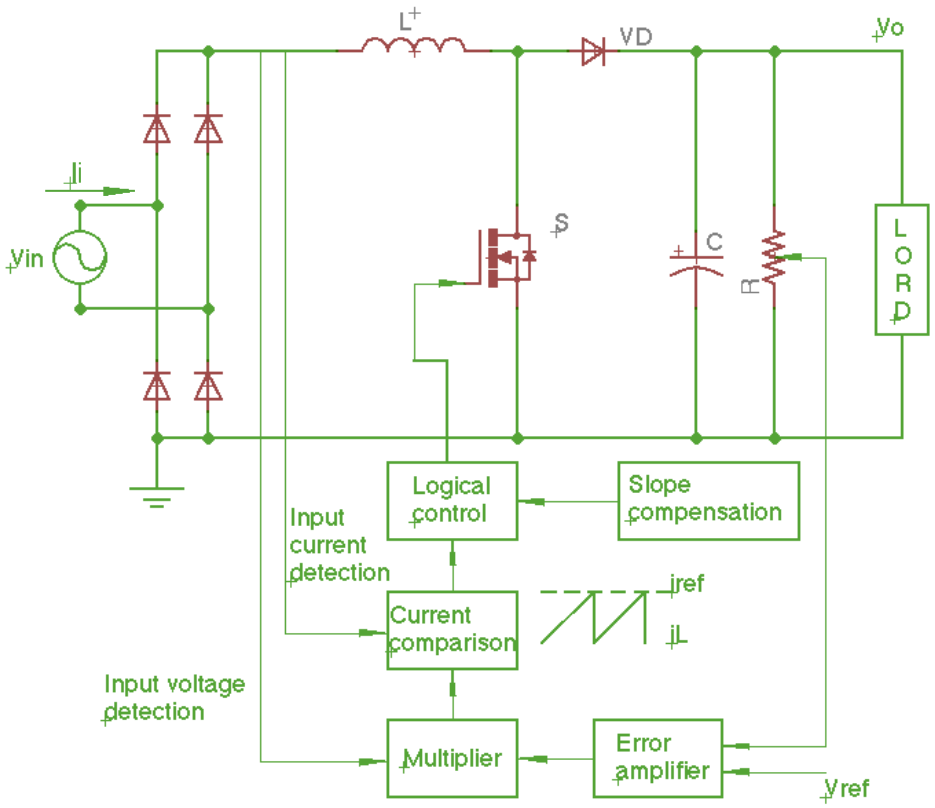


Fig.2.11(a) Peak current mode control PFC

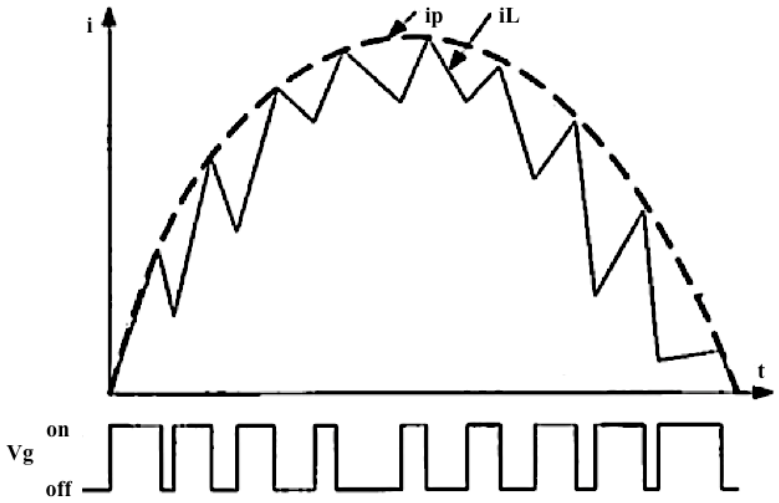


Fig.2.11(b) Peak current mode control inductor current waveform

(2) Hysteresis current control [15] [16]

Fig.2.12(a)-(b) shows the hysteresis current control Boost PFC circuit and the control waveform of switch S and inductor current i_L in half of the switching circle. Different from peak current control mode, the variable we take control in this control mode is the range of the inductor current. We multiply the input voltage signal with the feedback signal of the output voltage, then we will have two different current control reference signals which are same phase and same frequency with the input voltage. We call larger signal upper bound reference current loop signal and the smaller one lower bound reference current loop signal. We detect the inductor current and compare it with the two reference current signals. The control strategy is as follows:

- When the switch S is on, the inductor L will be charged, and the detected inductor current is compared with the upper bound reference current loop signal. And when the inductor current rises to the upper bound, the trigger logic control will cut off the switch S and the inductor starts discharging.
- When the inductor current falls to lower bound, the trigger logic control will turn on the switch and the inductor L gets charged.

In this control mode, the conducting time of switch S is constant, but the shutdown time varies. So the switching cycle is not constant. The bandwidth of hysteresis decides the size of the ripple, which can be constant or in proportion to instantaneous average current.

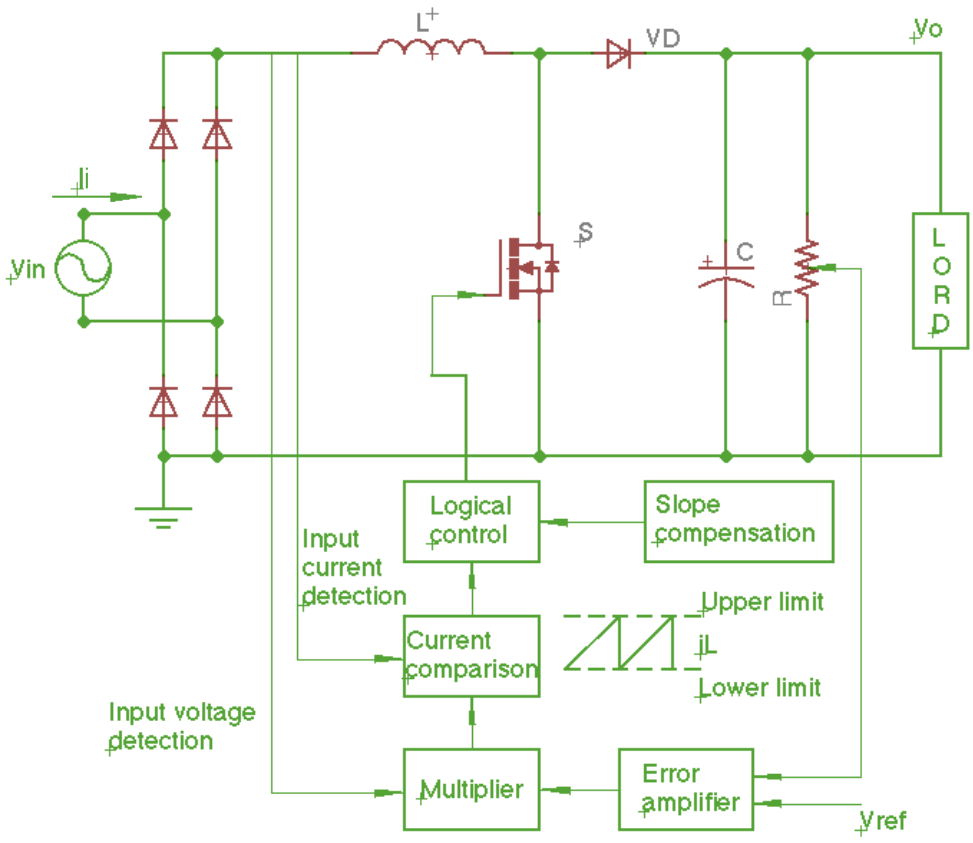


Fig.2.12(a) Hysteresis current control PFC

For Boost PFC, hysteresis current control is a simple control mode, because we have no extra modulation signal. And we can get wide current bandwidth and fast dynamic response. The disadvantage of this circuit is very obvious, that is, the load has large effects on the switch, so when we design the filter we need to consider the lowest switching frequency. Also the hysteresis bandwidth has large effect on switching frequency and system performance. Moreover, when source voltage approaches zero the difference between two reference signals is very small, so we always need some compensation for this circuit.

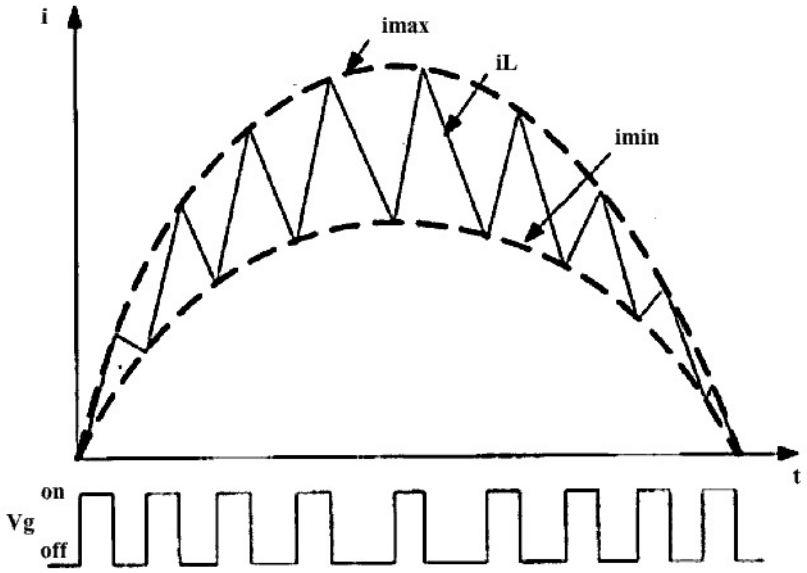


Fig.2.12(b) Hysteresis current control inductor current waveform

(3) Average current mode control

Fig.2.13(a) shows the schematic diagram of average current mode control. This kind of circuit is most widely used in PFC, and the inductor current waveform is shown in Fig.2.13(b). We multiply the rectified input voltage with amplified error signal of output voltage, and take the result as the reference signal. Through current loop regulation, we can control the average current and make it same phase with the input voltage. We detect the input current directly and then compare it with the reference current, and then the high frequency components will be average processed by the current error amplifier. Then we compare the amplified average current error with the sawtooth wave ramp and generate the switch driving signal, which decides the duty circle. So the current error will be eliminated in a fast speed [17].

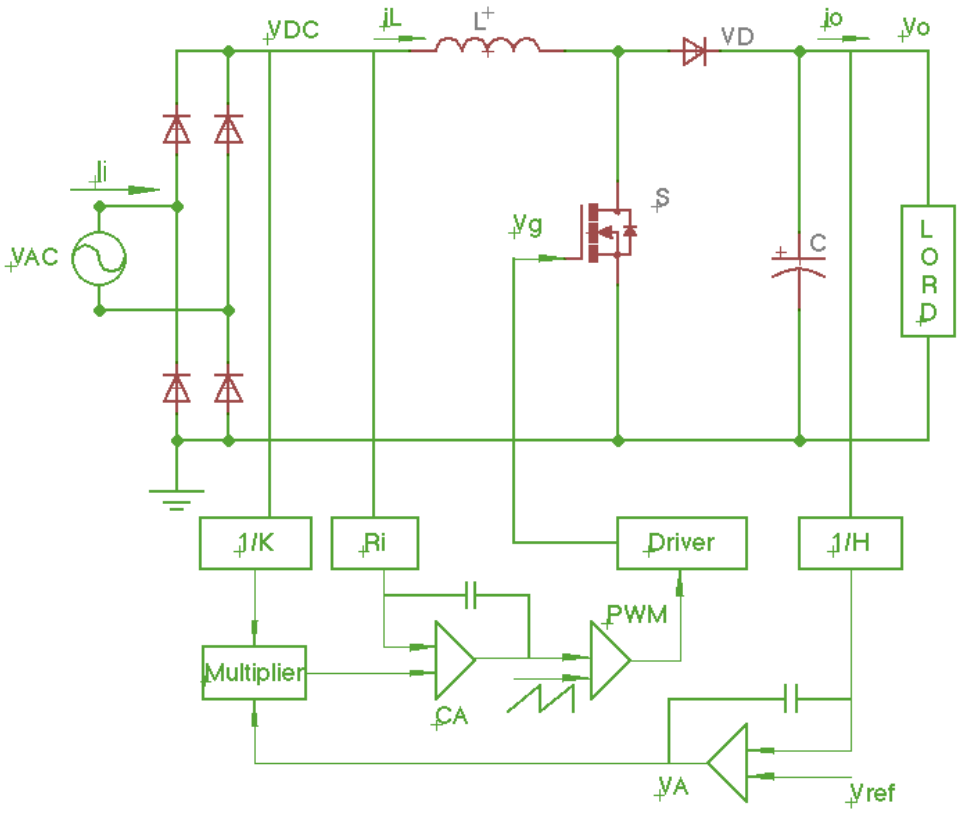


Fig.2.13(a) Average current mode control PFC

The advantage of average current mode control is that the variable is the average of input current, so the THD and EMI is small; it is not sensitive to noise; it can work under both CCM and DCM mode; and the switching frequency is constant so it is good for high power applications. And this is the most widely used control mode in PFC.

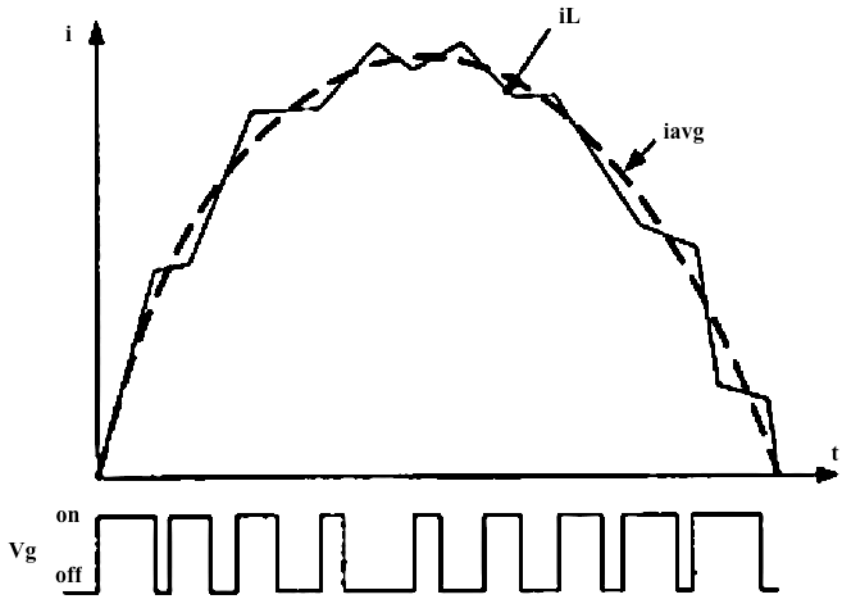


Fig.2.13(b) Average current mode control inductor current waveform

2.4 The Advantages and Disadvantages of Boost APFC

Advantages:

(1) The input current is continuous, and the EMI as well as the THD are small.

(2) It contains the input inductor, so there is less requirement for input filter. The input inductor can protect the main circuit from the high frequency transient impulse coming from power grid.

(3) The output voltage is larger than the peak of input voltage.

(4) The maximum voltage across the transistor switch S is smaller than the output voltage.

(5) It's easy to control the switch and the potential of the source is zero.

(6) It can work properly under a wide range of voltage and frequency.

Disadvantages:

(1) There is no insulation between the input and the output.

(2) If there is stray inductance in the loop composed by the switch S, diode D and the output capacitor C, there will be an overvoltage in the condition of 25-100KHz PWM frequency. So it is not safe for switch S.

Normally, boost APFC circuit is used for hundreds of watts to several kilowatts.

2.5 Summary

- In this chapter, the definition of power factor and the relationship between power factor and harmonic are described.
- Several common APFC main circuit topologies are listed, and their characteristics are compared and analyzed.
- The main circuit topology of several improved single-phase power factor correction is introduced, and the function of the circuit is analyzed.
- In this chapter, the control method of power factor correction technology is analyzed in detail, the principle of work is analyzed, and the advantages and disadvantages of each method and its application are pointed out.
- In the end, the advantages of APFC type Boost circuit are summarized.

Chapter 3: Design and simulation of the PFC boost converter

The design is based on the two-stage level 1 charging system in electric and hybrid electric vehicles. And the PFC circuit in the system is to correct the power factor and stabilize the voltage to the DC/DC stage. And the load is set as an equivalent resistor in this design. And there are several PFC topologies used in the market these days, but this design is based on conventional PFC circuit. And the main circuit is shown in Fig.3.1.

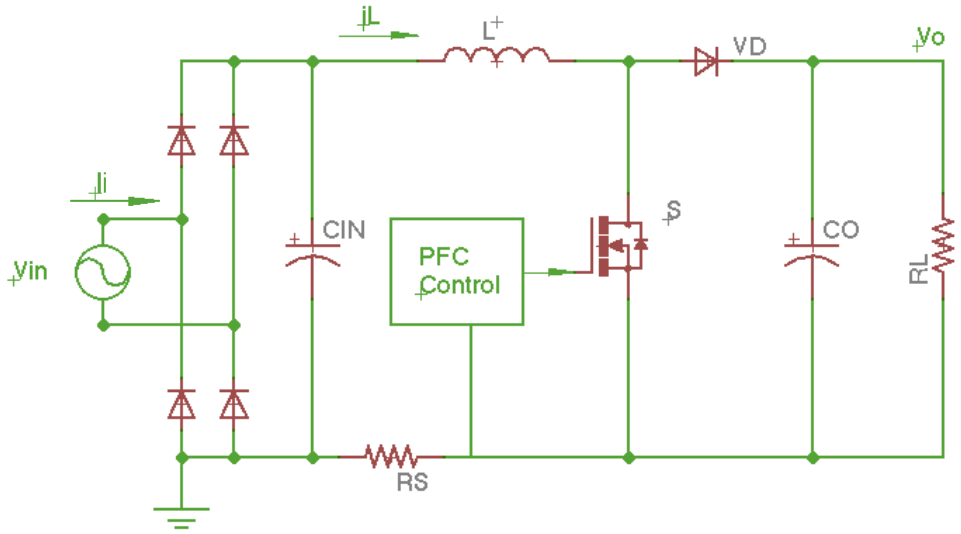


Fig.3.1 Conventional boost PFC circuit

3.1 System Main Circuit Design

3.1.1 Specifications

Determine the Operating Requirements for the Active Power Factor Corrector.

a. Rated output power P_o: 1.5kW

b. AC input voltage range: 85-140VAC

c. Grid frequency range: 60±1Hz

d. Output DC voltage U_o: 400V

e. Switch frequency f_{sw}: 50kHz

f. Efficiency η: >94%

3.1.2 Input filter capacitor selection [18]

The input filter capacitor is required to withstand input transient voltage as well as the superposition of the ripple voltage. The maximum high frequency ripple voltage ratio $r=\Delta V_L/V_L\approx0.02\sim0.08$, when considering the worst condition is the minimum input voltage. ΔV_L is the ripple voltage across the inductor, and V_L is the inductor voltage.

The formula for calculating the input filter capacitor is:

$$C_{in} \geq \frac{I_{rms}\bullet K_r}{V_{rms(min)}\bullet r\bullet \omega_s} \tag{3.1}$$

K_r is the ripple current coefficient, f_s is the switch frequency and $\omega_s=2\pi f_s$, $V_{rms(min)}$ is the minimum input voltage, I_{rms} is the rms value of the input current. Set Kr=0.2, r=0.05, f_s=50kHz, and we can get $C_{in}\geq2.64\mu F$. We select 3μF as the input filter capacitor.

3.1.3 Boost inductor selection [1]

The inductor is composed of a winding and a magnetic core, which plays the role of energy transfer, storage and filtering, and determines the magnitude of the high frequency ripple in the input current. The design of the inductor is crucial to the performance,

efficiency and function of the circuit, and whether the effect of the inductor can be satisfied.

When it is the minimum input current, current ripple is the maximum. In order to guarantee that the input current ripple meets the requirement in that situation, we need to calculate the inductor when the it is the minimum input voltage [19] [20].

$$L\frac{\Delta I_L}{DT_s} = V_{in} \tag{3.2}$$

$$L = \frac{V_{in}DT_s}{\Delta I_L} = \frac{V_{in}D}{f_s\Delta I_L} \tag{3.3}$$

In equations (3.2) and (3.3), L is the inductance, ΔI_L is the inductor ripple current, T_s is the switching period and D is the duty cycle.

a. Calculate the peak of the maximum input current:

$$I_{PK} = \frac{\sqrt{2}P_{in}}{V_{in(min)}} = \frac{\sqrt{2}\times 1500}{85} = 24.96(A) \tag{3.4}$$

In equation (3.4), P_{in} is the input power.

b. The maximum inductor current ripple ΔI_L allowed is normally set as 20% of the maximum peak inductor current:

$$\Delta I_L = 0.2I_{PK} = 0.2\times 24.96 = 5(A) \tag{3.5}$$

c. Calculate the duty cycle when the inductor current gets to the maximum peak. When the input voltage reaches the peak, the input current reaches the peak with the maximum ripple current. Therefore, we should calculate the duty cycle when it is the minimum input voltage:

$$D = \frac{V_o - \sqrt{2}V_{in(min)}}{V_o} = \frac{400 - \sqrt{2}\times 85}{400} = 0.7 \quad (3.6)$$

In equation (3.6), V_o is the output DC voltage.

d. At last, we can calculate the value of the boost inductor combining equation (3.3), (3.5) and (3.6):

$$L = \frac{\sqrt{2}V_{in(min)} \cdot D}{f_s \cdot \Delta I_L} = \frac{\sqrt{2}\times 85\times 0.7}{50\times 10^3 \times 5} = 0.44(mH) \quad (3.7)$$

3.1.4 Output capacitor selection

When selecting the output capacitor, the second harmonic current, the switching frequency ripple current, the DC output voltage, the output voltage ripple [21], and the hold-up time are considered. The total current through the output capacitor is the second harmonic of line current and the rms value of switching frequency ripple current. Usually we choose aluminum electrolytic capacitors that have long life, low leakage resistance, ability to resist large ripple current and work in a wide range.

There are two ways to design the output capacitance. The first one is to meet the requirement of the output ripple voltage, and the second one is to satisfy the hold-up time. In this design, we directly use the second method. And we set the hold-up time as 35ms and minimum output DC voltage as 350V [22].

$$C_o = \frac{2P_o \bullet \Delta t}{U_o^2 - U_{o(min)}^2} = \frac{2\times 1500\times 35\times 10^{-3}}{400^2 - 350^2} = 2.8(mF) \quad (3.8)$$

In equation (3.8), P_o is the output power, Δt is the hold-up time, $U_{o(min)}$ is the minimum output DC voltage.

3.1.5 Current sensing resistor selection

Normally there are two methods to sense the current, connecting a resistor in series in the line or using current transformer. Using sensing resistor will be cheaper than the other method, and it is mainly applied in low power and low current situations. So in this design, we use sensing resistor to detect the input current. The voltage across the sensing resistor will be modulated by the current loop and force the input current to be sinusoidal.

The dissipation power on sensing resistor should be below 10W, we set the power as 5W [18].

$$R_S = \frac{P_S}{I_{R(RMS)}^2} = \frac{P_S}{(I_{PK}/\sqrt{2})^2} = \frac{5}{(24.96/\sqrt{2})^2} = 0.016(\Omega) \quad (3.9)$$

In equation (3.9), P_s is the power dissipated on the sensing resistor, and $I_{R(RMS)}$ is the rms value of the current through the sensing resistor. For convenience, we select R_s to be 0.02Ω [22].

3.1.6 Power switch transistor and diodes selection [18]

When the switch transistor turns on, the diode reverse cutoff and the current flowing through the transistor is the inductor current, and the reverse voltage across the diode is output voltage. When the switch transistor turns off, the diode conducts forward. The voltage across the switch transistor is the output voltage, and the current flowing through the diode is the inductor current.

So, when selecting power switch transistor and diodes, the rated voltage must be greater than the output voltage, and the rated current must be greater than the maximum inductor current. We take the safety margin of voltage and current to be 1.2 and 1.5.

$$V_{rated} \geq 1.2V_o = 1.2\times400 = 480(V) \tag{3.10}$$

$$I_{rated} \geq 1.5I_{L(max)} = 1.5I_{PK} = 1.5\times24.96 = 37.44(A) \tag{3.11}$$

3.2 APFC Control Circuit Design

PFC circuit has the both the function of rectification and voltage stabilization, that is, the rectification requires the input power factor to be 1, and the voltage stabilization requires stable output voltage. Therefore, PFC circuit must be applied voltage feedback and current feedback simultaneously to form a dual loop control system. The outer loop is to keep the output voltage stable, and the inner loop shape the input current to make it a standard sinusoidal waveform with the same phase of the input voltage.

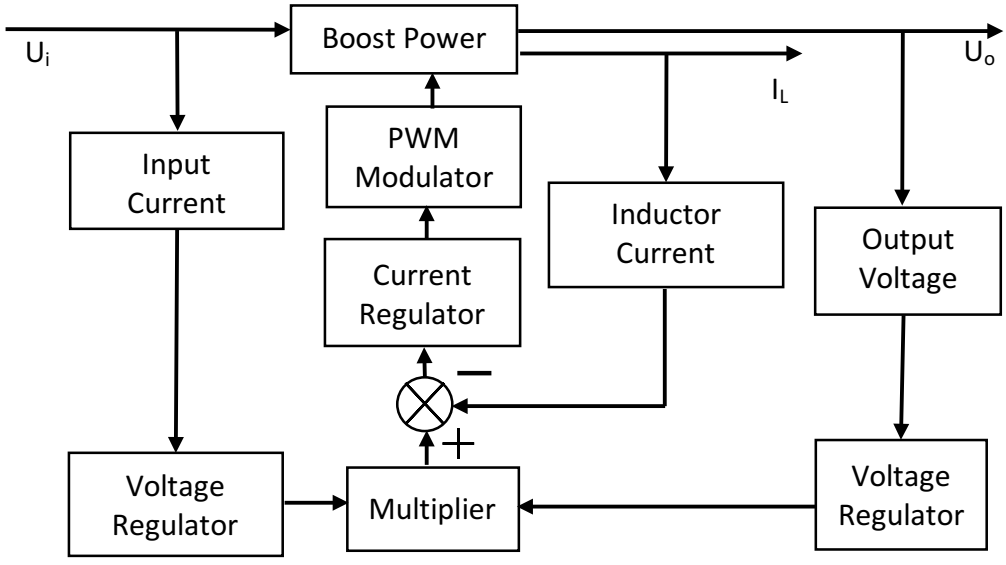


Fig.3.2 Control structure block diagram of PFC circuit

According to the above ideas, the control circuit of PFC can be drawn, and the control structure diagram is shown in Fig.3.2. In the figure, the boost power level represents the main circuit boost converter of PFC, of which the power device is controlled by the output signal conduction ratio (D) of the current controller, and operates in switch mode and achieve input current shaping and output voltage stabling.

Voltage regulator is used to improve the dynamic characteristics of the PFC output voltage. Its output signal U_e is multiplied by the instantaneously detected input voltage signal in the multiplier, and then divided by square of the input voltage rms value, then we constitute the reference current signal. After that, the reference current is compared with the instantaneously detected input current signal, and the result is processed by the PWM technology to achieve input current control to drive the switch.

3.2.1 Current control loop design for PFC circuit [1]

Current loop is the inner loop, which modulates the duty cycle of the power switch transistor, and force the input current to track the input voltage waveform. Because the input voltage is full-wave rectified waveform and contains rich harmonics, the current control loop must have enough bandwidth. While designing current control loop, we suppose the output voltage fully tracks the reference voltage, which is a constant value.

We can draw the ACM controlled current control loop as Fig.3.3. It consists of the current error amplifier, the pulse width modulator (PWM) and the power stage. In this figure, $G_{CEA}(s)$ represents the transfer function of the current error amplifier; $G_{PWM}(s)$ represents the transfer function of the pulse width modulator; and $G_P(s)$ represents the transfer function that the voltage across the sensing resistor R_s is controlled by the duty cycle D.

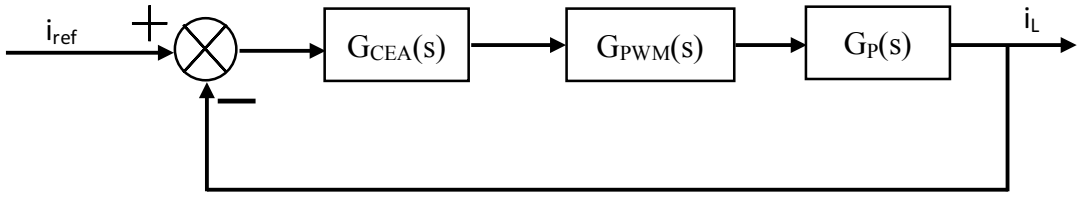


Fig.3.3 Current control loop structure

a. Power stage

In one switch cycle, the inductor voltage is:

$$L\frac{di_L}{dt} = U_i,\ switch\ on \tag{3.12}$$

$$L\frac{di_L}{dt} = U_i - U_o,\ switch\ off \tag{3.13}$$

According to the state space averaging technic, we can get:

$$I_L(s) = \frac{V_o \bullet D(s)}{S \bullet L} \tag{3.14}$$

And we can calculate the power stage transfer function:

$$G_P(s) = \frac{V_S(s)}{D(s)} = \frac{R_S \bullet I_L(s)}{D(s)} = \frac{R_S \bullet V_o}{s \bullet L} \tag{3.15}$$

b. Pulse width modulator

The principle of the PWM generator is shown as Fig.3.4.

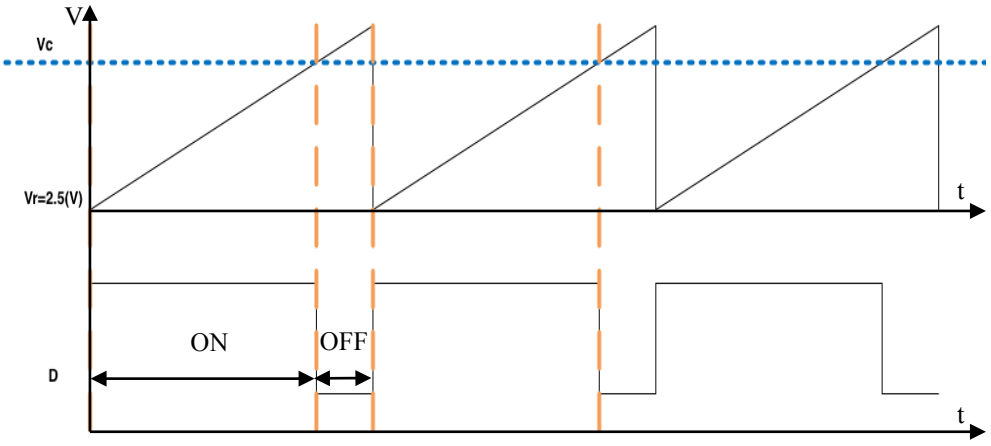


Fig.3.4 Pulse width modulator

The peak-peak voltage V_r of the sawtooth signal is set as 2.5V [23]. And the duty cycle is get from the calculation of V_r minus the output signal of the current error amplifier V_c. So we can get the transfer function:

$$G_{PWM}(s) = \frac{\Delta D}{\Delta V_c} = \frac{1}{V_r} \tag{3.16}$$

c. Current error amplifier

We use a PI controller to achieve the function of the current error amplifier [24]:

$$G_{CEA}(s) = k_{pc} + \frac{k_{ic}}{s} \tag{3.17}$$

So the open loop transfer function of the current loop is:

$$G_i(s) = G_{CEA}(s) \bullet G_{PWM}(s) \bullet G_P(s) \tag{3.18}$$

In order to give the current loop enough bandwidth to track the reference current, the open loop crossover frequency of the current loop is set 5kHz. And to make the system stable and have a proper respond speed, the phase margin is set 45˚ [25]. So we could write the two functions as below:

$$|\mathrm{G_i(s)}| = |\mathrm{G_{CEA}(s) \bullet G_{PWM}(s) \bullet G_P(s)}| = 1 \tag{3.19}$$

$$\angle G_i(s) = -180^\circ + 45^\circ \tag{3.20}$$

So we can calculate the parameters of the current loop PI controller, k_{pc}=2.16 and k_{ic}=6.79×10^4. And we can write the transfer function of the current error amplifier and the current control loop:

$$G_{CEA}(s) = 2.16 + \frac{6.79\times10^4}{s} \tag{3.21}$$

$$G_i(s) = \frac{R_s \bullet V_o}{s \bullet L \bullet V_r}\left(k_{pc} + \frac{k_{ic}}{s}\right) = \frac{0.02\times400}{s\times0.44\times10^{-3}\times2.5}\left(2.16 + \frac{6.79\times10^4}{s}\right) = \frac{17.28s+5.432\times10^5}{0.0011s^2} \tag{3.22}$$

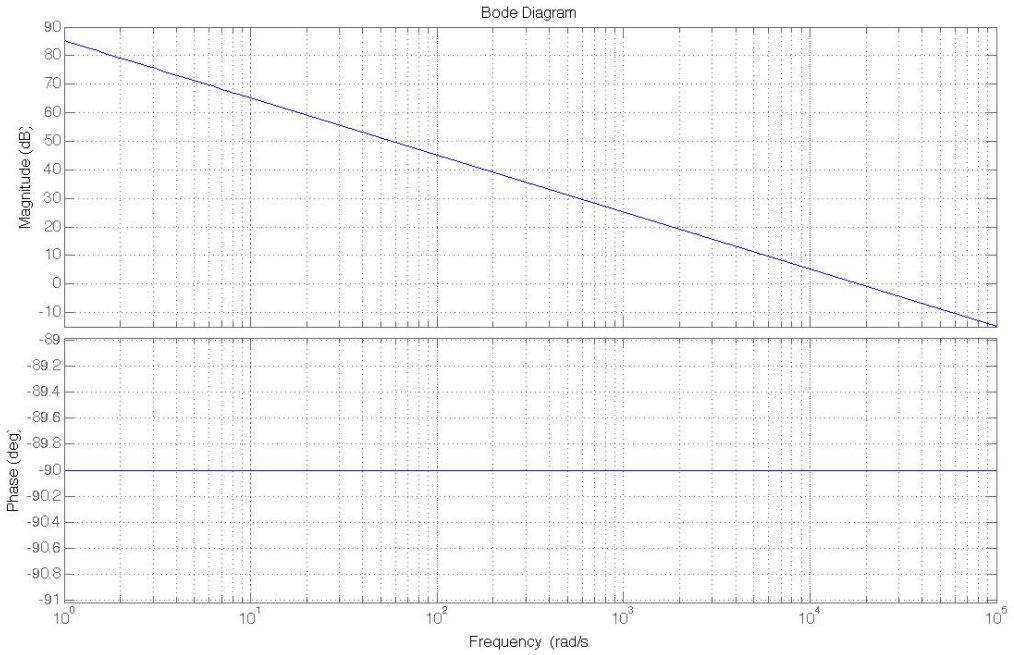


Fig.3.5 Bode diagram of the power stage

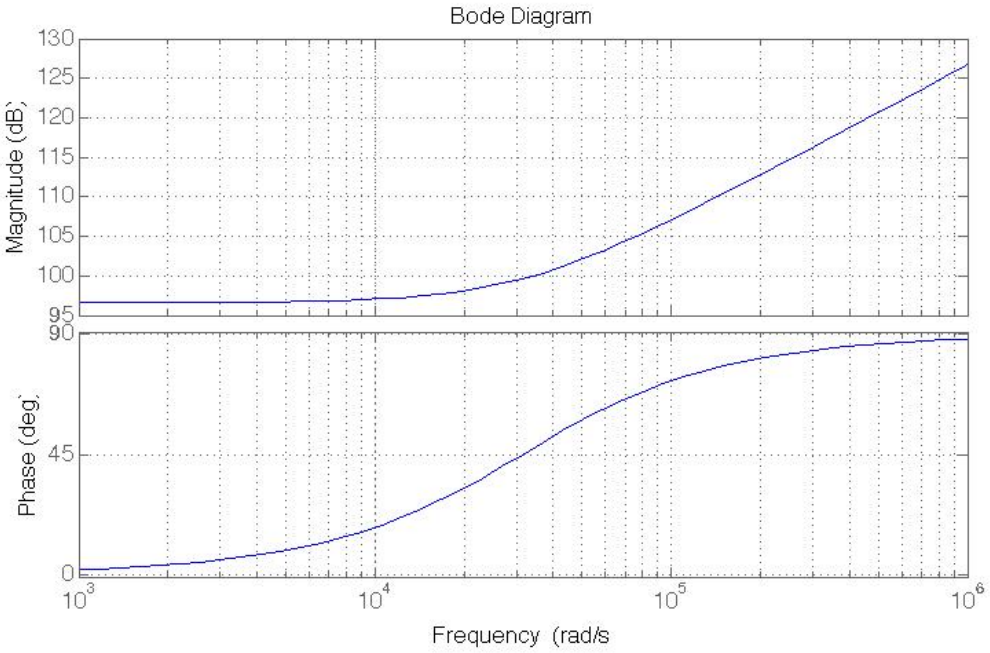


Fig.3.6 Bode diagram of the current error amplifier

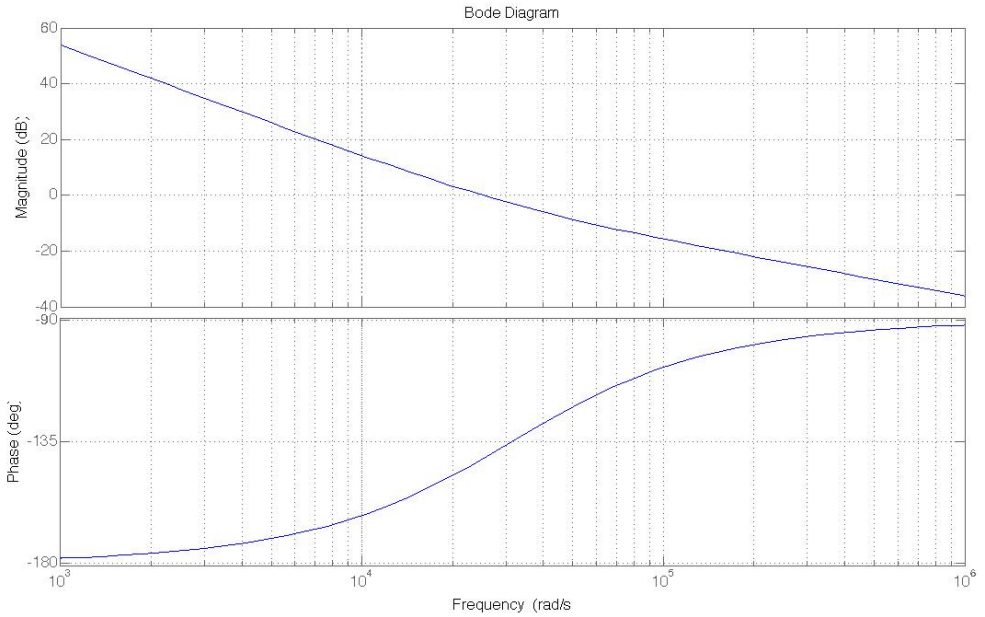


Fig.3.7 Bode diagram of the current open loop

From the simulation of MATLAB in Fig.3.5-3.7, we can see that when the $|G_p(s)|=1$, the crossover frequency of the power stage is around 2.86KHz. So the bandwidth of the power stage is too small and needs to be compensated, and it should be improved to around 5KHz. And after the signal going through the current error amplifier as designed, the magnitude of the current open loop $|G_i(s)|=1$ at 4.8KHz. So the design meets the requirement of the compensation and keeps the system stable.

3.2.2 Voltage control loop design for PFC circuit [1]

Voltage control loop is the outer loop, which provides the reference current signal for the inner current control loop, and stable the output DC voltage of the PFC system by modulate the magnitude of the reference current signal. In the study of the voltage control loop, we could ignore the input voltage ripple in one switch cycle because the speed of the outer loop is much slower than the inner loop. And to simplify the analysis, we suppose that inductor current fully tracts the reference current, that is the inner closed current control loop is ideal, and also we suppose the output power is constant and the input average power equals the output average power.

The voltage control loop can be drawn as Fig.3.8, and it includes the voltage error amplifier, the closed current control loop and the boost stage. In the figure below, $G_{VEA}(s)$ represents the transfer function of the voltage error amplifier; the constant 1 represents the inner closed current control loop; and $G_{bst}(s)$ represents the transfer function of the boost stage.

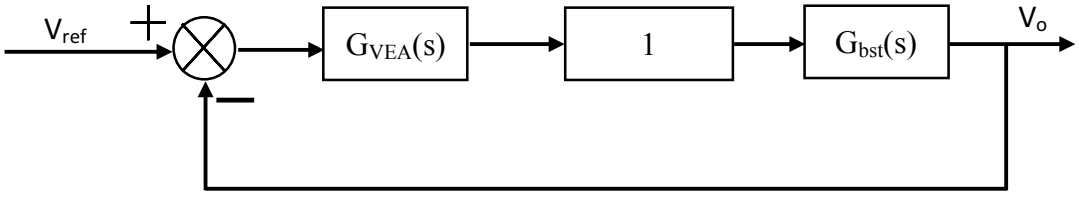


Fig.3.8 Voltage control loop structure

a. Boost stage

The function of the i_{ref} can be write as below [25]:

$$i_{ref} = \frac{K_m \bullet K_{in} \bullet V_v \bullet |v_i|}{V_{ff}^2} = \sqrt{2}\frac{K_m \bullet K_{in} \bullet V_v \bullet V_{i(rms)} \bullet |sin\omega t|}{V_{ff}^2} \quad (3.23)$$

In the function, K_m is the current control loop coefficient and equals to constant 1; K_{in} is the input voltage sampling coefficient and is set 1/80 [23]; $V_{i(rms)}$ is the rms value of the input voltage; V_v is the output signal of the voltage error amplifier; V_{ff} is the feedforward voltage, and the denominator V_{ff}^2 of the equation makes the input power not vary with the change of the input voltage.

And we also have the equation of the inductor current i_L:

$$i_L = \sqrt{2}\frac{K_i \bullet P_i \bullet |sin\omega t|}{V_{i(rms)}} \quad (3.24)$$

K_i is the input current sampling coefficient; P_i is the input average power. And then we have:

$$P_i = P_o = V_o \bullet I_o \quad (3.25)$$

P_o is the output average power; V_o and I_o are the steady state components of the output voltage and current.

Then according to the equations above, we have:

$$V_o \bullet I_o = \frac{K_m \bullet K_{in} \bullet V_v}{K_i} \left(\frac{V_{i(rms)}}{V_{ff}}\right)^2 = K_{bst} \bullet V_v \tag{3.26}$$

$$K_{bst} = \frac{K_m \bullet K_{in}}{K_i} \left(\frac{V_{i(rms)}}{V_{ff}}\right)^2 \tag{3.27}$$

K_{bst} is a constant, and V_o, I_o and V_v are DC operating points of the voltage loop.

Considering the output of the PFC circuit, we have:

$$i_o = \frac{P_o}{u_o} + C\frac{du_o}{dt} \tag{3.28}$$

Because P_o is assumed constant, we solve the equation in small-signal analysis method:

$$\frac{K_{bst} \bullet \tilde{u}_v}{V_o} = C\frac{d\tilde{u}_o}{dt} \tag{3.29}$$

In the equation above, $\tilde{u}_o$ and $\tilde{u}_v$ are small-signal perturbations. So using Laplace transformation we can get the transfer function of the voltage control boost stage:

$$G_{bst}(s) = \frac{\tilde{u}_o}{\tilde{u}_v} = \frac{K_{bst}}{C \bullet V_o \bullet s} \tag{3.30}$$

b. Voltage error amplifier

The input frequency of the system is 60Hz, so the second harmonic output voltage ripple is at 120Hz. In order to restrain the affection of the second harmonic output voltage ripple to the current control loop, the voltage open loop crossover frequency is normally set 1/10 of the second harmonic frequency. So in this design, the crossover frequency is set 12Hz.

And the transfer function of the voltage error amplifier is written as [18]:

$$G_{VEA} = \frac{k_v}{1 + {}^{s}/_{\omega_{cv}}} \tag{3.31}$$

So the open loop transfer function of the voltage loop is:

$$G_v(s) = K_{vs} \bullet G_{VEA}(s) \bullet G_{bst}(s) \tag{3.32}$$

K_{vs} is the output voltage sampling coefficient and is set 1/80 [23].

Also to make the system stable and well responded, the phase margin of the open voltage loop is set 45˚ [25]. Therefore, we can get:

$$|G_v(s)| = |K_{vs} \bullet G_{VEA}(s) \bullet G_{bst}(s)| = 1 \tag{3.33}$$

$$\angle G_v(s) = -180^\circ + 45^\circ \tag{3.34}$$

Then we calculate the parameters of the voltage error amplifier, and get k_v=2.8149 and ω_{cv}=75.4 rad/s. After calculation we also get $K_{bst}=\frac{1/80}{0.02}(\sqrt{2}\pi/4)^2$=4840. And we can write the transfer function of the voltage error amplifier and the voltage control loop:

$$G_{VEA} = \frac{2.8149}{1+{}^{s}/_{75.4}} \tag{3.35}$$

$$G_v(s) = \frac{1}{80} \bullet \frac{k_v}{1+{}^{s}/_{\omega_{cv}}} \bullet \frac{K_{bst}}{C \bullet V_o \bullet s} = \frac{1}{80} \bullet \frac{2.8149}{1+{}^{s}/_{75.4}} \bullet \frac{4840}{2.8\times10^{-3}\times400s} = \frac{1.36\times10^4}{89.6s+1.188s^2} \tag{3.36}$$

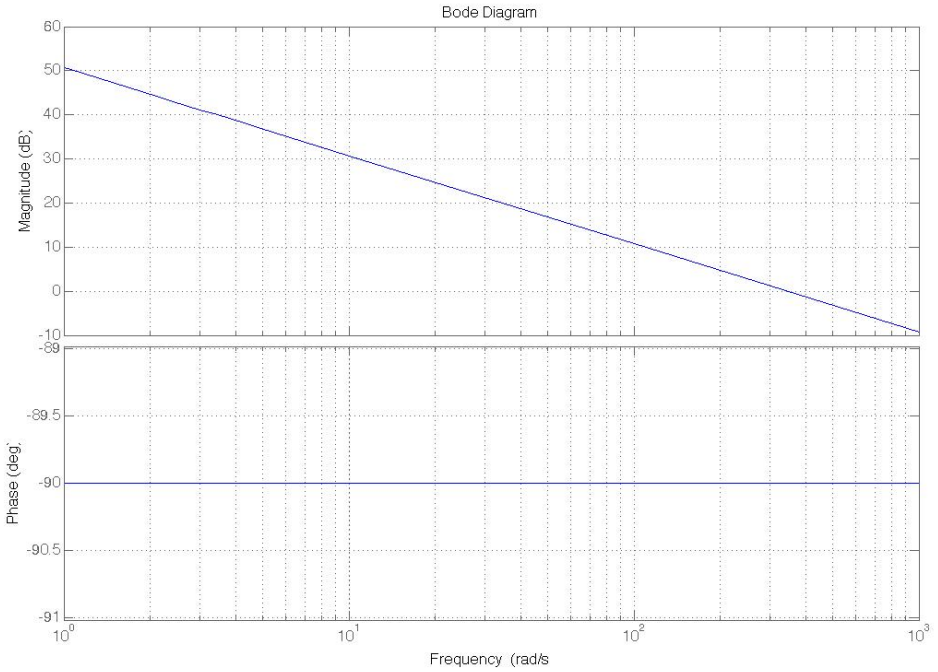


Fig.3.9 Bode diagram of the boost stage

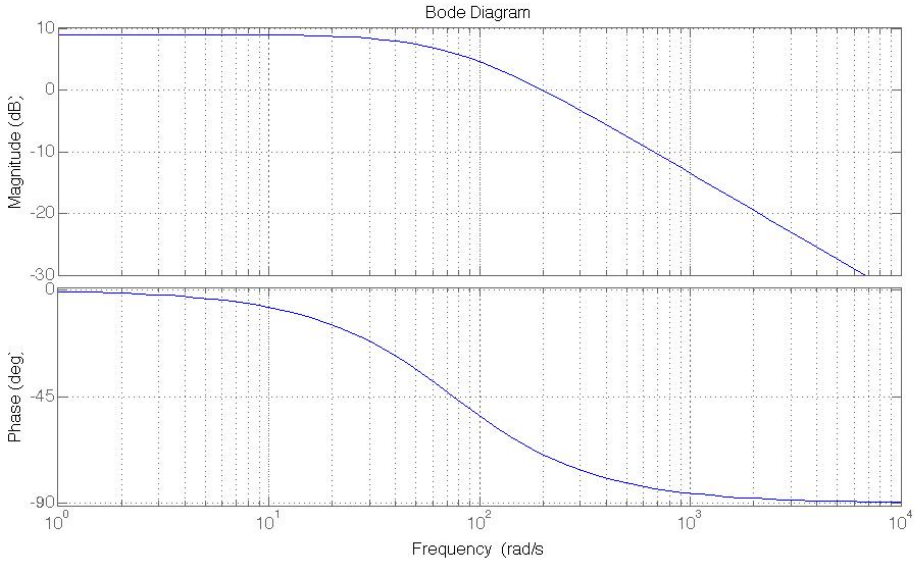


Fig.3.10 Bode diagram of the voltage error amplifier

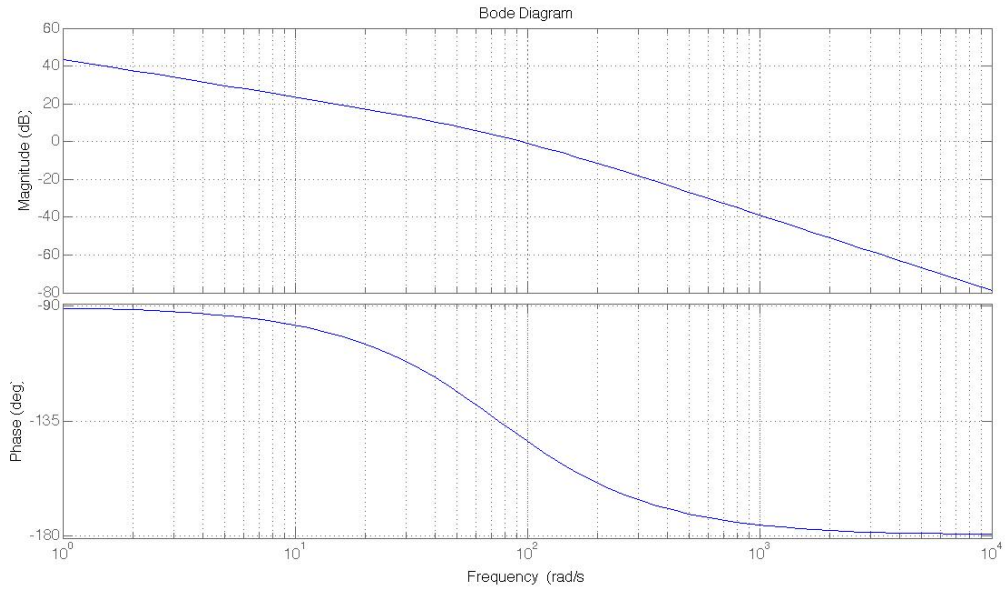


Fig.3.11 Bode diagram of the voltage open loop

According to the simulation results of MATLAB in Fig.3.9-3.11, we can get that when the $|G_{bst}(s)|=1$, the crossover frequency of the boost stage is around 340Hz. So the bandwidth of the voltage loop is too large and needs to be compensated, and it should be improved to around 12Hz. Then taking the designed current error amplifier into the voltage loop, the magnitude of the voltage open loop $|G_v(s)|=1$ at around 13Hz. So the design meets the requirement of the compensation and stabilizes the system.

3.3 System Simulation and Results Analysis

According to the calculations above, I use Simulink to build the circuit and run the simulation. The circuit consists of an internal current loop and an external voltage loop, and the two loops are connected together by a multiplier. There are two input ports of the

multiplier. One is the AC sinusoidal half wave signal, which is the rectified given AC sinusoidal wave signal; the other one is the difference of the output DC bus sampling voltage and the reference voltage, and the difference will go through a first order process and the amplitude will be limited. The output of the multiplier is also an AC sinusoidal half wave signal, whose amplitude is regulated by the output DC bus voltage. The multiplier output works as the reference value of the current loop, and it is compared with the inductor sampling current and outputs the result to the PI controller and get adjusted, and at last PWM drive signal can be generated and control the operation of the MOSFET.

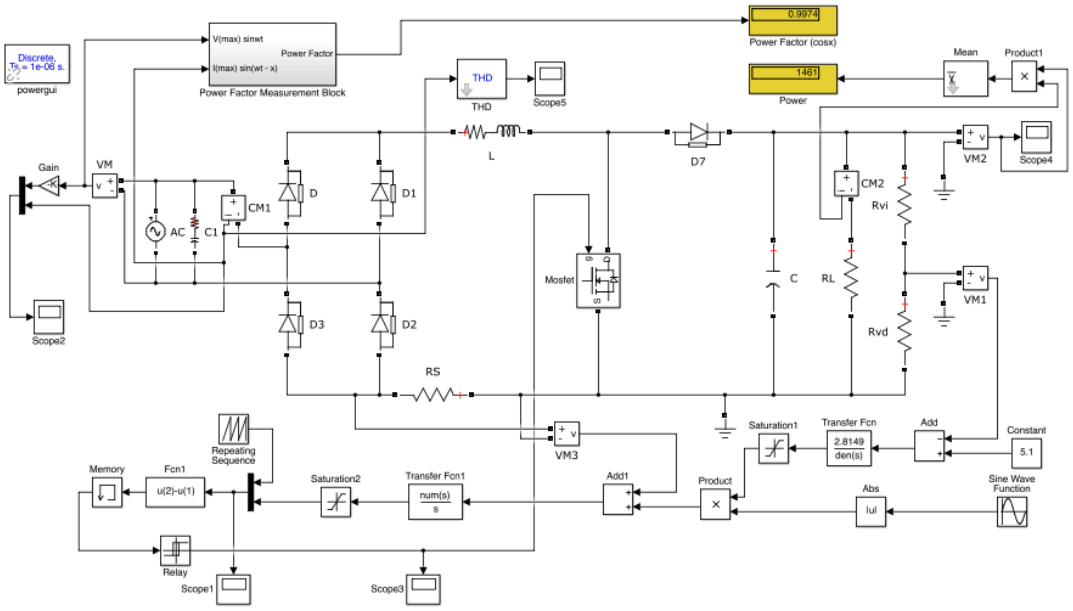


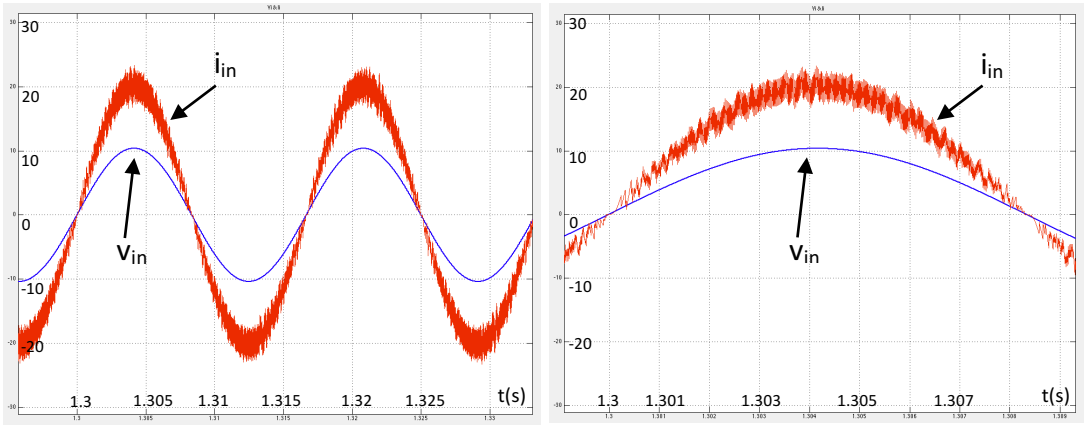
Fig.3.12 APFC simulation mode schematic in Simulink

The parameters applied in the simulation: input AC voltage is 110V/60Hz, the boost inductor L=0.44mH, the output filter capacitor C=2.8mF, and the load resistor R_L=106Ω.

Fig.3.13 shows the contrast diagram of the input AC current and the input AC voltage waveforms. The input voltage signal is scaled by 1/15 so that it is easier to compare. From the figure we can obvious see that the input current waveform is standard sinusoidal waveform and is nearly the same phase with the input voltage waveform. The input current peak value is around 20A, and the current ripple peak-to-peak value is below 5A, which satisfy the design objective.

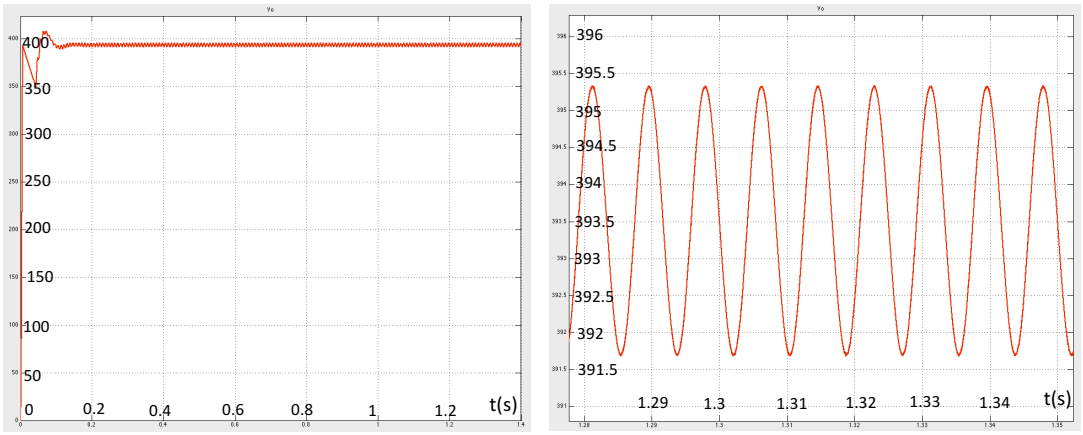
Fig.3.14 shows the output DC voltage waveform. The average value of the output voltage is about 393.5V, and the voltage ripple peak-to-peak value is below 4V, which meets the requirements of the design.

Through the output power calculating component that I designed in the Simulink, it is shown that the output power is 1461W, which is very close to the design goal. And through the power factor calculating component that I designed in the Simulink, the power factor is shown as 99.74%, which means the PFC circuit greatly improves the power factor of the boost circuit. The frequency spectrum diagram is shown in Fig.3.15, and the THD of the input current is 7.05%, which is largely reduced.



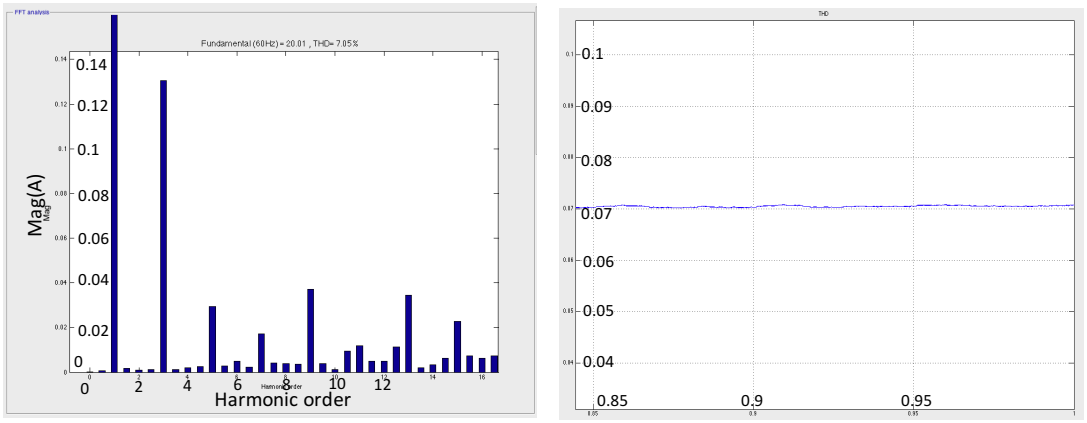
(a) (b)

Fig.3.13 Input current and input voltage waves



(a) (b)

Fig.3.14 Output DC voltage wave



(a) (b)

Fig.3.15 Diagram of the input current (a) frequency spectrum, (b) THD

Fig.3.16-3.19 shows the input voltage and input current waveforms and frequency spectrum of a group of different input voltage. Through the figures we can see that the input current waveforms are standard sinusoidal waveforms and are strictly the same phase with the input voltage waves.

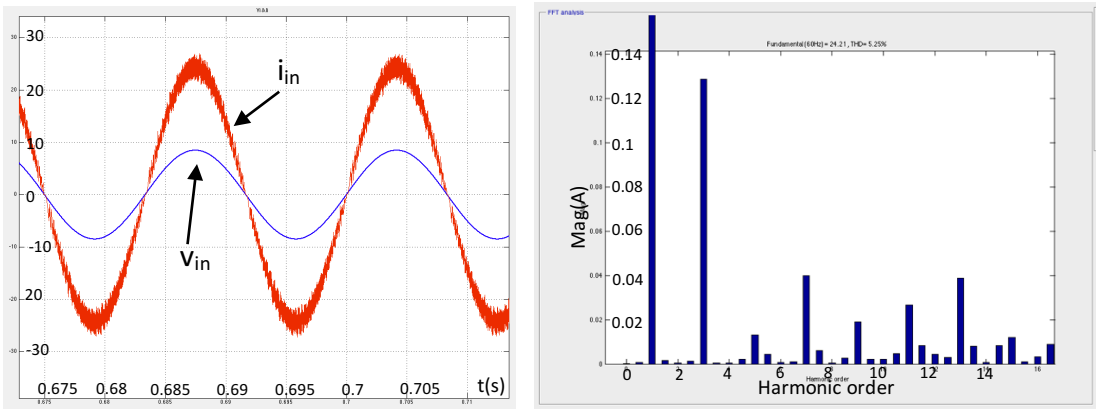


Fig.3.16 When the input voltage is 90V, the diagram of (a) the input voltage and current (b) frequency spectrum

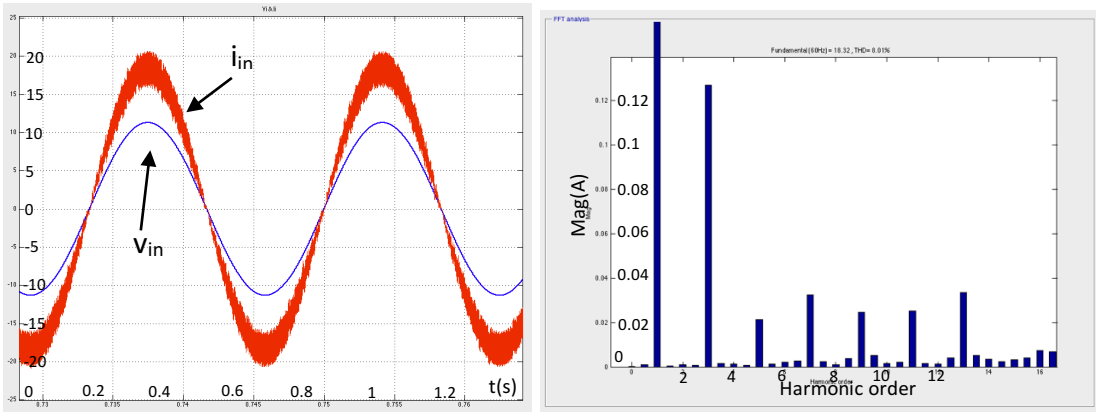


Fig.3.17 When the input voltage is 120V, the diagram of (a) the input voltage and current (b) frequency spectrum

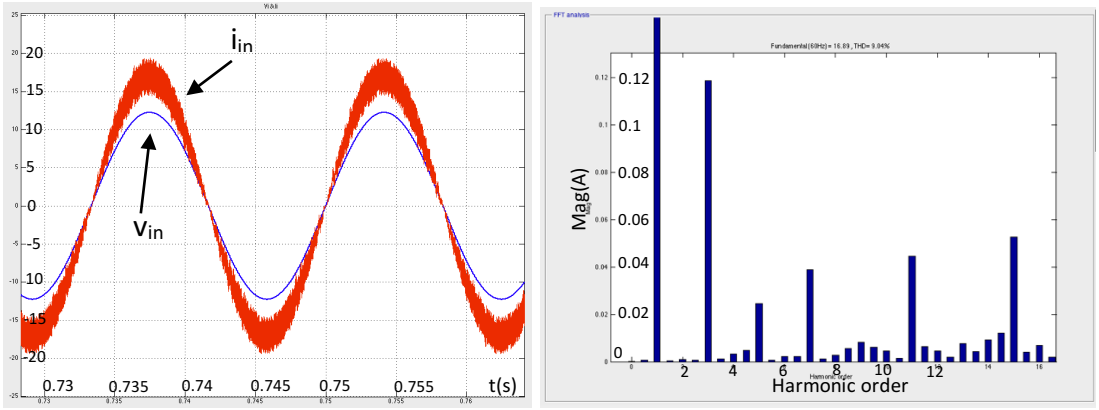


Fig.3.18 When the input voltage is 130V, the diagram of (a) the input voltage and current (b) frequency spectrum

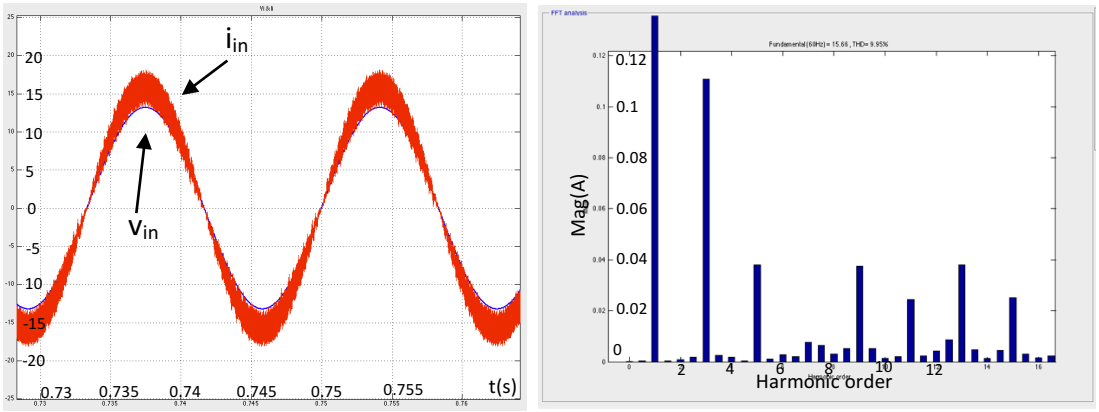


Fig.3.19 When the input voltage is 140V, the diagram of (a) the input voltage and current (b) frequency spectrum

Table 3.1-3.4 shows the output DC voltage, PF value and harmonic currents in the range of AC input voltage at 1500W as well as in 110VAC input voltage at different input power. We can see that when the input power is too small (below 1kW), the THD is too large and the system is not working in the perfect status. And in other conditions, the magnitude of the harmonic currents satisfies the requirement. And the result of the power factor correction is pretty good.

Table 3.1: Output DC voltage and PF value in the range of AC input voltage at 1500W

Input voltage (V)	Input current (A)	Output DC voltage (V)	Power Factor (%)	Input power (W)
90	17.38	393.5	99.66	1460

110	14.15	393.5	99.74	1461
120	12.96	393.6	99.67	1462
130	11.94	393.5	99.58	1461
140	11.08	393.5	99.48	1461

Table 3.2: Odd harmonic current values in the range of AC input voltage at 1500W

Input current (A)	3^{rd} harmonic component (A)	5^{th} harmonic component (A)	7^{th} harmonic component (A)	9^{th} harmonic component (A)	THD (%)
17.38	0.13	0.01	0.04	0.02	5.25
14.15	0.13	0.03	0.02	0.04	7.05
12.96	0.13	0.02	0.03	0.02	8.01
11.94	0.12	0.02	0.04	0.01	9.04
11.08	0.11	0.04	0.01	0.04	9.95

Table 3.3: Output DC voltage and PF value in 110VAC input voltage at different input power

Input voltage (V)	Input current (A)	Output DC voltage (V)	Power Factor (%)	Input power (W)
110	5.21	402	98.13	506.71
110	7.04	400.7	98.96	702.8
110	9.72	398	99.46	990.03
110	14.15	393.5	99.74	1461
110	16.6	391	99.81	1720
110	18.25	389.2	99.84	1895
110	22.29	385.3	99.89	2318
110	26.19	381.2	99.92	2725

Table 3.4: Odd harmonic current values in 110VAC input voltage at different input power

Input current (A)	3rd harmonic component (A)	5th harmonic component (A)	7th harmonic component (A)	9th harmonic component (A)	THD (%)
5.21	0.07	0.04	0.03	0.04	19.33
7.04	0.07	0.03	0.02	0.03	14.30
9.72	0.1	0.03	0.02	0.03	10.28
14.15	0.13	0.03	0.02	0.04	7.05
16.6	0.15	0.03	0.02	0.04	6.00
18.25	0.17	0.04	0.02	0.04	5.45
22.29	0.2	0.03	0.02	0.05	4.49
26.19	0.23	0.04	0.02	0.05	3.88

3.4 Summary

The boost PFC circuit can work properly for the first level charging of electric vehicle. It can operate in a range of input voltage and input power. And it achieves the shaping of the input current waveform and stabilizing the output voltage. The input voltage range is 85-140 VAC, the input power range is 1-3kW, the power factor stays more than 99%, and THD stays below 10%.

Conclusion

The power factor and harmonic pollution influence to the grid from the power electronic devices is an increasingly prominent problem. For the research and design of power electronic devices, it has been more and more focused on the whole operation characteristics of the system other than only considering the output characteristics of the system. To build the PFC circuit in EV charging system, not only we need to consider the output voltage, current features and adaptability to load, but also we should take into account the input features to reduce adverse effects.

In my design, the PFC circuit is applied in EV first level two-stage charging system, which is mostly operated in the common house hold circuit. Therefore, I set the rated output power 1.5kW, output DC voltage around 400V, frequency 60±1Hz. And also I set AC input voltage range 85-140VAC, and the available output power range around 1-3kW. First I calculated and designed the main circuit of the PFC system, which will meet the requirements of the input and output voltage as well as output power. After that I successively designed the inner current control loop and the outer voltage control loop. To complete the design of the dual-loop controller, I calculated the transfer functions of each loop and discussed the magnitude of the open loop transfer function and the phase margin of each loop. Then, I run the complete system in Simulink and got figures and data of some signals and do the comparison and analysis. Finally, through the research of the results of the simulation, I verified that this PFC system works in the specified conditions properly. In the results, we can see that under the first level charging

specifications, the PFC system will offer more than 99% PF for the circuit, and reduce the THD to less than 10%. It totally achieves the goal of rectifying, high input power factor, boosting voltage, stabilizing the output voltage and small ripples. Therefore, this design could be applied in the EV first level charging.

Still, there are things to be improved. Adding soft switch technology will do good to this PFC system, which can make it a very simple, efficient, high efficiency, high reliability way to achieve the transformation of electrical energy.

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An Active Boost Type APFC Power Management Circuit

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Abstract: With the development of wireless sensors, wireless technology and micro-electromechanical systems, the micro power supply system attracts people more attention. And since mechanical vibration energy is widely distributed in nature and is subject to less restrictive environmental factors, it is gradually becoming a new study object for energy collection. At present, according to the latest study, the Magnetic Shape Memory Alloys (MSMA) under the condition of external stress will change its own magnetic permeability, and we can obtain a large induced voltage by the mutative magnetic flux through the induction coil. This article proposes an active boost type APFC (Active Power Factor Correction) power management circuit, the APFC circuit aims to allow the input current waveform to follow the input voltage waveform so as to improve power factor and this circuit here mainly includes AC / DC rectifier, control circuit and capacitor energy storage module. By doing circuit simulation, it is found that in the case of the input voltage amplitude and frequency changing, the input current will follow the changes and both of them have almost the same phase, finally this circuit can achieve the goal to charge the capacitor stably. At last, this article summarizes that this circuit can boost the output power of the vibration energy, reduce energy loss, and increase the power factor to 0.90 by using power meter.

Key Words: power factor correction, power management, energy harvesting, simulation

1 INTRODUCTION

Vibration energy is a new energy resource that is discovered by scientists in recent years, which is ubiquitous in the environment. Vibration energy harvesting is a process that converts mechanical vibrations into electrical energy and it mainly includes electromagnetic induction technology, piezoelectric technology or smart materials technology etc. Magnetic Shape Memory Alloys (MSMA) as the smart materials emerging in recent years, it compared with other smart materials has these characteristics such as a greater rate of deformation, convenient control, high induced output voltage[1-2]. However, the output voltage and current are relatively still small and can't supply the load directly. So, this paper presents a power management circuit based on power factor correction, aiming to collect more vibration energy, improve the efficiency of energy supply and finally power to the load.

2 MSMA VIBRATION ENERGY HARVESTING WORKING-PRINCIPLE

MSMA as a new smart material will produce martensitic transformation under an external applied stress and magnetic field, its deformation and magneto-electric conversion efficiency are far greater than the piezoelectric materials and Terfenol-D materials, at the same time its maximum linear deformation and bending deformation rate respectively can reach 10% and 18% [3]. According to the Villari effect, we find that the shape memory feature of MSMA is reversible and this material not only can produce distortion and output force in the magnetic, but also can produce large electromagnetic signal changes by the magnetic energy varying. So, as above, we can convert mechanical energy into electromagnetic energy by the feature of MSMA material. MSMA energy harvesting principle is shown in Fig. 1.

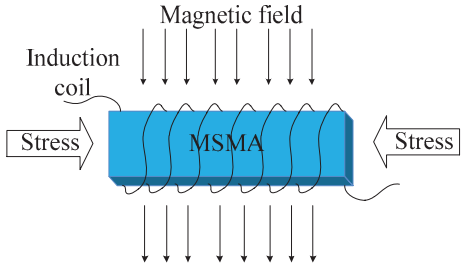

Fig 1. MSMA energy harvesting schematics

When magnetic shape memory alloys (MSMA) which is in a constant magnetic field is applied by a certain force, the magnetization of the alloy material will change, causing the magnetic flux through the inside of induction coils changed. According to Faraday law of electromagnetic induction, induced voltage will appear in the induction coils and the voltage is $V = -\frac{\partial B}{\partial t} NS$, V is the induced voltage in the coil; B is the magnetic flux density passing

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through the inside of the coil; N is the turns of coils; S is the sectional area of the coil.

3 BOOST TYPE APFC POWER MANAGEMENT CIRCUIT DESIGN

In most energy harvesting circuits, the AC voltage in induced coils should be first rectified, the rectifier circuit is shown in Fig. 2. In Fig. 2, the circuit connects an electrolytic capacitor C_{in} which stores power when the circuit working, and R_L represents the load. However, this circuit has a drawback that only when the input voltage exceeds the capacitor voltage, it will produce the input current as shown in Fig. 3. Thus, this circuit can cause severe distortion of the current waveform and generate low power factor about 0.5 or lower [4]. Taking into account the current in this circuit is not continuous and the circuit has current dead zone and low power factor, we use an active boost power factor correction circuit for power management.

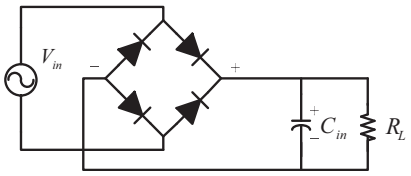


Fig 2. Full bridge rectifier filter circuit

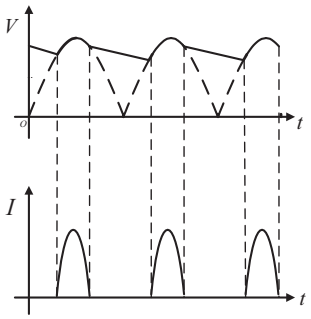


Fig 3. Full bridge rectifier voltage – current

3.1 Boost Type APFC Circuit Introduction

First, The APFC circuit presented in this paper adds a DC chopper circuit between the rectifier circuit and filter capacitor, as shown in Fig.4. When the MOS switch Q_1 turns on, current passes through the inductor L_1 and the switch Q_1. Before the inductor L_1 is not saturated, current gradually increases and the electric energy is stored in inductor L_1 . When the MOS switch Q_1 turns off, inductor L_1 is in a discharged state, current passes through the inductor L_1 and diode D_1, the capacitor C_{in} is in charging state which is equivalent to that power V_{in} and inductor L_1 together supply power to capacitor C_{in} and load R_L [5]. In summary, we can control the MOS switch on or off to ensure the persistence of the current circuit, eliminate current dead zone, increase the fundamental current RMS and the total current RMS ratio and improve the circuit power factor in the end.

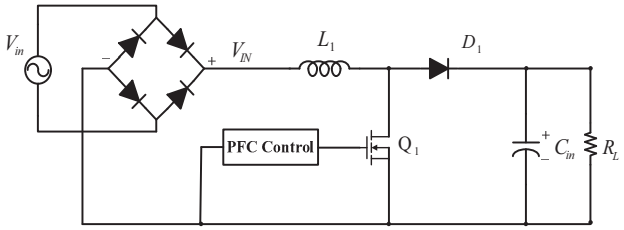


Fig 4. Boost type APFC circuit

3.2 Boost type APFC circuit modal analysis

By analyzing the APFC circuit in Section 3.1, it has found that the input voltage in the circuit has full-wave rectified waveform. It is known from the literature [6], the current in each switching cycle passing through the inductor is:

$$i_s\left(t^{'},t\right)=i_{L1}\left(t^{'},t\right)=\frac{V_{IN}t^{'}}{L_1}\left|\sin wt\right|,\ 0<t^{'}<dT_s \quad (1)$$

In (1), T_s is switching cycle, d is the MOS switch Q_1 conduction ratio, $t^{'}$ denotes the turn-on time in each switching cycle. The average current every cycle passing through the inductor L_1 and the input current RMS are respectively (2) and (3) as follows.

$$I_{L1}(t)=\frac{1}{2}i_{L1}\left(t^{'},t\right)\times(1-\Delta)=\frac{V_{IN}dT_s}{2L_1}(1-\Delta)\left|\sin wt\right| \quad (2)$$

$$I_{rms}=\frac{d^2\cdot T_S\cdot V_p}{2L_1}\frac{\sqrt{Z}}{\sqrt{\pi}} \quad (3)$$

In (2) and (3), Δ and Z are respectively:

$$\Delta=1-d\frac{m_{\min}}{m_{\min}-\left|\sin wt\right|} \quad (4)$$

$$Z=\frac{2m_{\min}^4}{m_{\min}^2-1}\left(\frac{m_{\min}^2+m_{\min}-1}{m_{\min}^2}+\frac{2}{m_{\min}\sqrt{m_{\min}^2-1}}\cdot\left(\frac{\pi}{2}-arctg\left(\frac{-1}{\sqrt{m_{\min}^2-1}}\right)\right)\right) \quad (5)$$

$m_{\min}$ denotes the minimum DC voltage ratio.

In addition, the average input power of this boost type APFC circuit in half cycle of the input voltage can be expressed as:

$$P_{IN}=\frac{V_{IN}^2d^2T_S}{2\pi L_1}\int_0^{\pi}\frac{\sin^2 wt}{1-\frac{1}{\mathrm{m}_{\min}}\sin wt}d(wt)=\frac{V_{IN}^2d^2T_S}{2\pi L_1}f(\mathrm{m}_{\min}) \quad (6)$$

In (6), $f(\mathrm{m}_{\min})=\int_0^{\pi}\frac{\sin^2 wt}{1-\frac{1}{\mathrm{m}_{\min}}\sin wt}d(wt)$.

In the case of ignoring the input voltage distortion, the input power factor is:

$$PF = \frac{P_{IN}}{I_{rms} \cdot V_{rms}} = \frac{\sqrt{2}}{\sqrt{\pi}} \cdot \frac{f(\mathrm{m}_{\min})}{\sqrt{Z}} \tag{7}$$

Therefore, in order to ensure the boost type APFC circuit presented in this article have a high power factor, we need to make it work in discontinuous conduction mode (DCM). In this mode, the switch conduction ratio is fixed and the output voltage in this circuit can be expressed as:

$$V_0 = \frac{1}{1-d} V_{IN} \tag{8}$$

3.3 The control circuit of APFC design

As shown in Section 3.2, the key of the power factor correction is to control the switch-off time effectively. After above analysis, when MOS switch Q_1 turns on, current I passes through the inductor L_1 and MOS switch Q_1 and the current is rising. When the MOS switch Q_1 turns off, current I passes through the inductor L_1 and diode D_1 and finally charges the capacitor C_{in}, but note that the current is decreasing during this time, as shown in Fig. 5. In Fig. 5, the half wave of sine represents V_{in}, the saw-tooth waveform shows the wave of current I during the MOS switch is on or off, the square wave represents the trigger pulse applies to the MOS switch Q_1 that can control Q_1 to be on or off. To improve the power factor of this energy harvesting circuit and guarantee the continuous current, it's necessary to determine the point in time that the switch is on and off. As seen from Fig. 5, the times that the current is reduced to zero and reaches the peak are two key time points. When the current is reduced to zero, MOS switch Q_1 should be on. When the current reaches peak, the current of inductor L_1 is saturated, MOS switch Q_1 should be off and the current passes toward capacitor C_{in} and charges it.

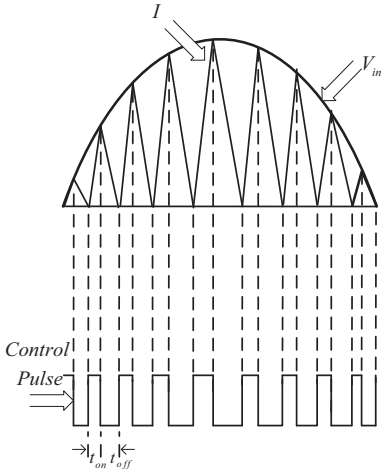


Fig 5. The control pulse diagram of MOS switch

As the APFC circuit simulation schematic shown in Fig. 6, in the comparator U1A, the positive input terminal voltage is the voltage across the resistor R5, the inverse input terminal voltage is equal to the voltage across resistor R3. When the positive input terminal voltage is greater than the inverse input terminal voltage, the comparator U1A output is high level, otherwise it is low level [7]. The section behind the comparator U1A is a RS trigger composed of two NAND gates, the voltage on a terminal of the NAND gate U2A is equal to the voltage across resistor R3 and the other terminal of the NAND gate U2A connects to a terminal of NAND gate U3A. The function of comparator U1A and RS trigger is to control the MOS switch Q_1 to be on or off. The operating mode of control circuit is as follows: (1) when MOS switch Q_1 is on, the current is rising during the time t_{on} and the inductor L_1 voltage is increasing. Then, when the inverse input terminal voltage in U1A is less than the positive terminal voltage, the comparator output is high level and the NAND gate U2A output is low level that is less than the turn-on voltage of MOS switch Q_1. So MOS switch Q_1 is off, the circuit current passes toward the capacitor C_{in} and charges it. (2) When MOS switch Q_1 is off, the circuit current is in the time t_{off} and the value is decreasing, the voltage across the capacitor C_{in} is rising, but the voltage across inductor L_1 is falling. Then, when the value of current is close to zero, the comparator U1A output is low level and the output voltage of U2A in RS trigger is high level that is higher than the turn-on voltage of MOS switch Q_1. So MOS switch is on. Due to that the inverse terminal input voltage is equal to the voltage across the resistor R5, which using the resistor R4 and R5 to divide rectified voltage, so the time t_{on} is fixed theoretically, the only changing time is t_{off} which represented that the inductor discharges. Therefore this control circuit is also called a fixed on-time control circuit. During this control circuit working, the current waveform is represented by the voltage across R3 which value is equal to 1k Ω.

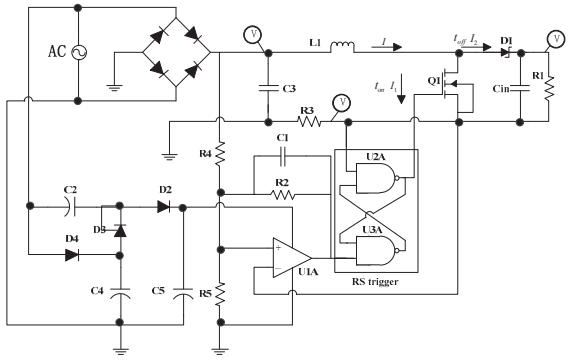
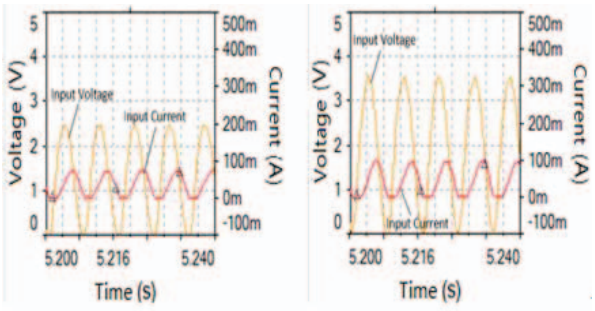


Fig 6. The APFC circuit simulation schematic

3.4 CIRCUIT SIMULATION RESULTS

Fig. 7 shows the input voltage waveform and the input current waveform when the input voltage is respectively 2.8V and 3.6V. Please note that the size of the input current is represented by a resistor voltage of R3. As shown in Fig. 7, the APFC circuit can make the phase and wave of input

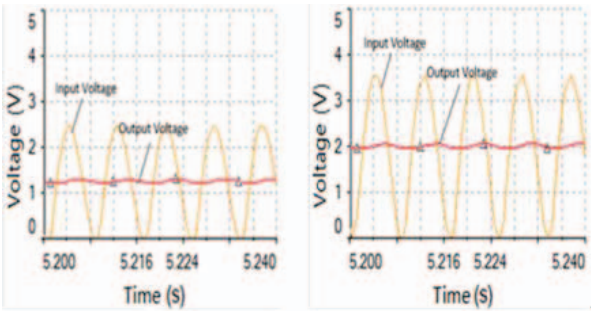
current and input voltage to be consistent. At the same time, the input current can well track input voltage.



(a) Voltage and current waveforms when the input voltage is 2.8V. (b) Voltage and current waveforms when the input voltage is 3.6V.

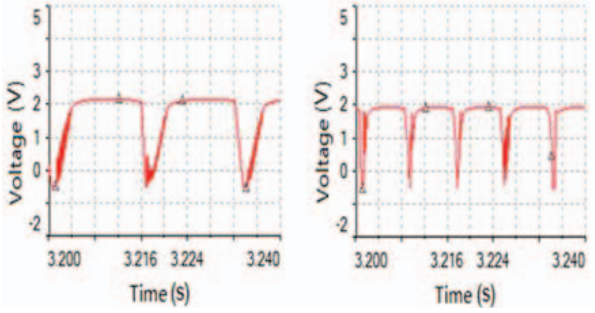
Fig 7. Input current waveform at different input voltage

In addition, Fig. 8 is the output current waveform at different input voltages. As seen in Fig. 8(a), when input voltage is 2.8V, the output voltage is about 1.6V. As seen in Fig.8 (b), when input voltage is 3.6V, the output voltage is about 2V. Fig. 9 is the MOS switch on-off voltage waveform. As shown in Fig. 9, when the frequency of input voltage changes, the MOS switch on-off time also changes. But relative to the changes of frequency, we can think the on-off time is fixed. So this circuit operates in a fixed on-off time critical mode which can improve power factor well.



(a) Voltage waveform when the input voltage is 2.8V (b) Voltage waveform when the input voltage is 3.6V

Fig 8. Output voltage waveform at different input voltages



(a) Voltage waveform when MOS switch is on and the input voltage frequency is 30Hz (b) Voltage waveform when MOS switch is on and the input voltage frequency is 60Hz

Fig 9. Voltage waveform when MOS switch is on in different Frequencies

4 RESULTS OF EXPERIMENTAL CIRCUIT

Fig.10 shows the MSMA vibration energy harvesting platform. By applying the induced voltage in coils to the APFC circuit, the induced voltage peak is about 2.8V at 30Hz frequency, we can get the waveform of input current represented by the voltage of resistor R3 and the input voltage, as shown in Fig. 11(a). Under the above conditions, we also can get the MOS switch on-off voltage waveform, as shown in Fig. 11(b). We can know from Fig. 11 that the phase of input current consists with the phase of input voltage, the capacitor is continuously charged and the output voltage in circuit is maintained at 1.56V which is basically consistent with the theoretical results. In addition, we have measured the power factor in this actual circuit that can reach 0.90 by using power meter.

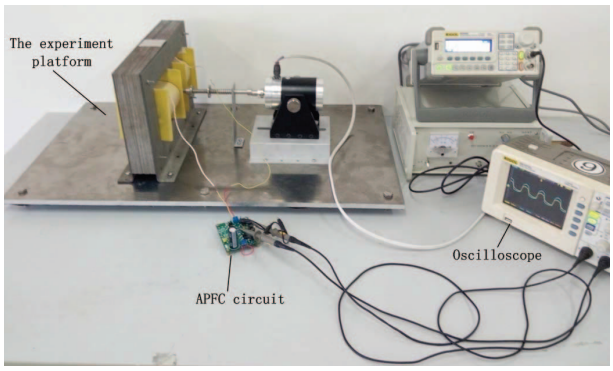
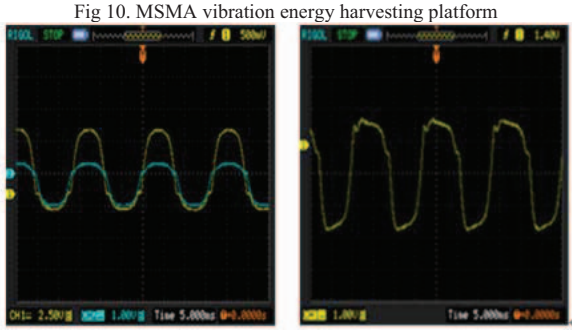
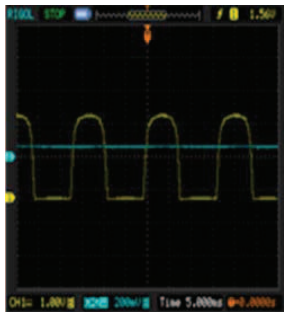


Fig 10. MSMA vibration energy harvesting platform



(a) Voltage and current waveforms when the input voltage is 2.8V (b) Voltage waveform when MOS switch is on and the input voltage



(c) Output voltage waveform when the input voltage is 2.8V

Fig 11. The waveform of input voltage, input current and MOS switch turn-on voltage in experiment

5 CONCLUSION

This paper presents a power management circuit based on power factor. By using APFC control circuit to open or close MOS switch, we can guarantee the continuous current existing in this circuit so that we are able to eliminate

current dead zone, reduce circuit energy loss and improve power factor to 0.9 which is less than 0.5 before. In addition, through circuit experiments, we find that the input current can follow the input voltage changes in case of the input voltage amplitude and frequency changing. Finally, this APFC circuit design establishes foundation for the next controlling capacitor discharging and designing external battery circuit.

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(v_L positive and i_L positive), forward regenerative braking (v_L positive and i_L negative), reverse direction (v_L negative and i_L negative), and reverse regenerative braking (v_L negative and i_L positive).

Key Points of Section 5.8

- With proper switch control, the four-quadrant converter can operate and control flow in any of the four quadrants. For operation in the third and fourth quadrants, the direction of the load emf E must be reversed internally.

5.9 SWITCHING-MODE REGULATORS

Dc converters can be used as switching-mode regulators to convert a dc voltage, normally unregulated, to a regulated dc output voltage. The regulation is normally achieved by PWM at a fixed frequency and the switching device is normally BJT, MOSFET, or IGBT. The elements of switching-mode regulators are shown in Figure 5.16. We can notice from Figure 5.2b that the output of dc converters with resistive load is discontinuous and contains harmonics. The ripple content is normally reduced by an LC filter.

Switching regulators are commercially available as integrated circuits. The designer can select the switching frequency by choosing the values of R and C of frequency oscillator. As a rule of thumb, to maximize efficiency, the minimum oscillator period should be about 100 times longer than the transistor switching time; for example, if a transistor has a switching time of 0.5 μs, the oscillator period would be 50 μs, which gives the maximum oscillator frequency of 20 kHz. This limitation is due to a switching loss in the transistor. The transistor switching loss increases with the switching frequency and as a result the efficiency decreases. In addition, the core loss of inductors limits the high-frequency operation. Control voltage v_c is obtained by comparing the output voltage with its desired value. The v_{cr} can be compared with a sawtooth voltage v_r to generate the PWM control signal for the dc converter. There are four basic topologies of switching regulators [33, 34]:

1. Buck regulators
2. Boost regulators
3. Buck–boost regulators
4. Cúk regulators

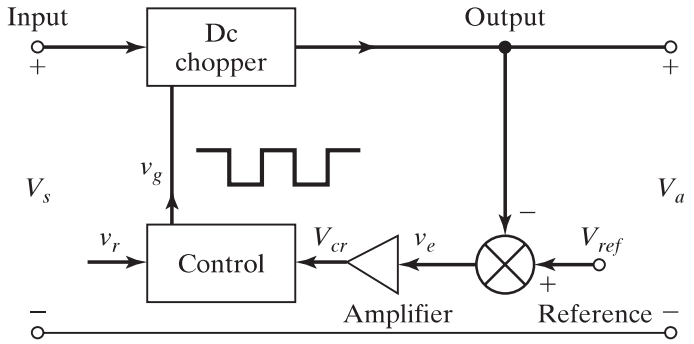


FIGURE 5.16
Elements of switching-mode regulators.

5.9.1 Buck Regulators

In a buck regulator, the average output voltage V_a is less than the input voltage, V_s—hence the name "buck," a very popular regulator [6, 7]. The circuit diagram of a buck regulator using a power BJT is shown in Figure 5.17a, and this is like a step-down converter. Transistor Q_1 acts as a controlled switch and diode D_m is an uncontrolled switch. They operate as two single-pole-single-through (SPST) bidirectional switches. The circuit in Figure 5.17a is often represented by two switches as shown in Figure 5.17b. The circuit operation can be divided into two modes. Mode 1 begins when transistor Q_1 is switched on at $t = 0$. The input current, which rises, flows through filter inductor L, filter capacitor C, and load resistor R. Mode 2 begins when transistor Q_1 is switched off at $t = t_1$. The freewheeling diode D_m conducts due to energy stored in the inductor, and the inductor current continues to flow through L, C, load, and diode D_m. The inductor current falls until transistor Q_1 is switched on again in the next cycle. The equivalent circuits for the modes of operation are shown in Figure 5.17c. The waveforms for the voltages and currents are shown in Figure 5.17d for a continuous current flow in the inductor L. It is assumed that the current rises and falls linearly. In practical circuits, the switch has a finite, nonlinear resistance. Its effect can generally be negligible in most applications. Depending on the switching frequency, filter inductance, and capacitance, the inductor current could be discontinuous.

The voltage across the inductor L is, in general,

$$e_L = L\frac{di}{dt}$$

Assuming that the inductor current rises linearly from I_1 to I_2 in time t_1,

$$V_s - V_a = L\frac{I_2 - I_1}{t_1} = L\frac{\Delta I}{t_1} \tag{5.52}$$

or

$$t_1 = \frac{\Delta I\, L}{V_s - V_a} \tag{5.53}$$

and the inductor current falls linearly from I_2 to I_1 in time t_2,

$$-V_a = -L\frac{\Delta I}{t_2} \tag{5.54}$$

or

$$t_2 = \frac{\Delta I\, L}{V_a} \tag{5.55}$$

where $\Delta I = I_2 - I_1$ is the peak-to-peak ripple current of the inductor L. Equating the value of ΔI in Eqs. (5.52) and (5.54) gives

$$\Delta I = \frac{(V_s - V_a)t_1}{L} = \frac{V_a t_2}{L}$$

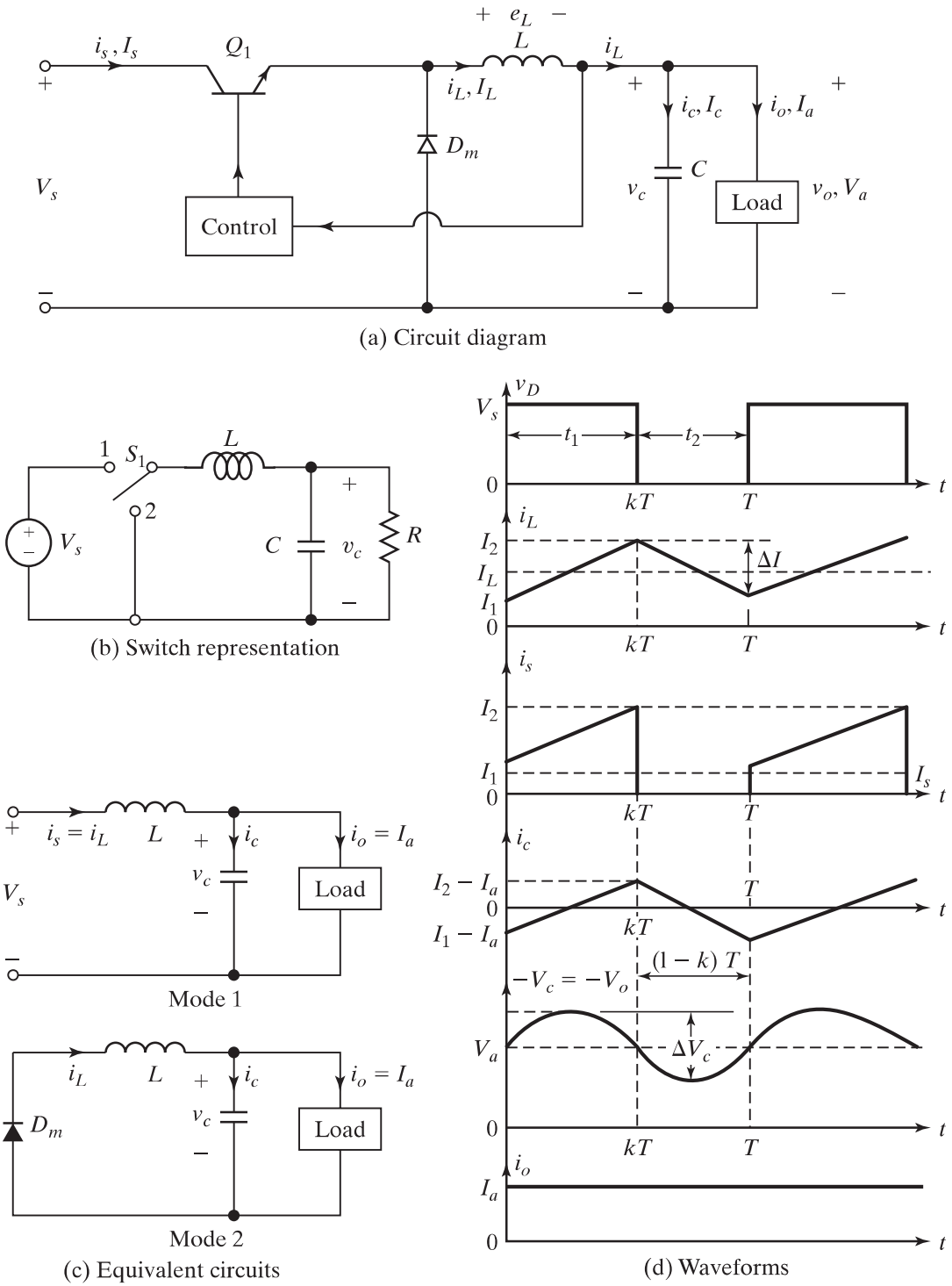


FIGURE 5.17

Buck regulator with continuous i_L.

Substituting $t_1 = kT$ and $t_2 = (1 - k)T$ yields the average output voltage as

$$V_a = V_s \frac{t_1}{T} = kV_s \tag{5.56}$$

Assuming a lossless circuit, $V_s I_s = V_a I_a = kV_s I_a$ and the average input current

$$I_s = kI_a \tag{5.57}$$

Peak-to-peak inductor ripple current. The switching period T can be expressed as

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta I\, L}{V_s - V_a} + \frac{\Delta I\, L}{V_a} = \frac{\Delta I\, L V_s}{V_a(V_s - V_a)} \tag{5.58}$$

which gives the peak-to-peak ripple current as

$$\Delta I = \frac{V_a(V_s - V_a)}{fLV_s} \tag{5.59}$$

or

$$\Delta I = \frac{V_s k(1 - k)}{fL} \tag{5.60}$$

Peak-to-peak capacitor ripple voltage. Using Kirchhoff's current law, we can write the inductor current i_L as

$$i_L = i_c + i_o$$

If we assume that the load ripple current Δi_o is very small and negligible, $\Delta i_L = \Delta i_c$. The average capacitor current, which flows into for $t_1/2 + t_2/2 = T/2$, is

$$I_c = \frac{\Delta I}{4}$$

The capacitor voltage is expressed as

$$v_c = \frac{1}{C}\int i_c\, dt + v_c(t = 0)$$

and the peak-to-peak ripple voltage of the capacitor is

$$\Delta V_c = v_c - v_c(t = 0) = \frac{1}{C}\int_0^{T/2} \frac{\Delta I}{4}\, dt = \frac{\Delta I\, T}{8C} = \frac{\Delta I}{8fC} \tag{5.61}$$

Substituting the value of ΔI from Eq. (5.59) or (5.60) in Eq. (5.61) yields

$$\Delta V_c = \frac{V_a(V_s - V_a)}{8LCf^2 V_s} \tag{5.62}$$

or

$$\Delta V_c = \frac{V_s k(1 - k)}{8LCf^2} \tag{5.63}$$

Condition for continuous inductor current and capacitor voltage. If I_L is the average inductor current, the inductor ripple current $\Delta I = 2I_L$.

Using Eqs. (5.56) and (5.60), we get

$$\frac{V_S(1-k)k}{fL} = 2I_L = 2I_a = \frac{2kV_s}{R}$$

which gives the critical value of the inductor L_c as

$$L_c = L = \frac{(1-k)R}{2f} \tag{5.64}$$

If V_c is the average capacitor voltage, the capacitor ripple voltage $\Delta V_c = 2V_a$. Using Eqs. (5.56) and (5.63), we get

$$\frac{V_s(1-k)k}{8LCf^2} = 2V_a = 2kV_s$$

which gives the critical value of the capacitor C_c as

$$C_c = C = \frac{1-k}{16Lf^2} \tag{5.65}$$

The buck regulator requires only one transistor, is simple, and has high efficiency greater than 90%. The *di/dt* of the load current is limited by inductor L. However, the input current is discontinuous and a smoothing input filter is normally required. It provides one polarity of output voltage and unidirectional output current. It requires a protection circuit in case of possible short circuit across the diode path.

Example 5.5 Finding the Values of *LC* Filter for the Buck Regulator

The buck regulator in Figure 5.17a has an input voltage of $V_s = 12\,\text{V}$. The required average output voltage is $V_a = 5\,\text{V}$ at $R = 500\,\Omega$ and the peak-to-peak output ripple voltage is 20 mV. The switching frequency is 25 kHz. If the peak-to-peak ripple current of inductor is limited to 0.8 A, determine (a) the duty cycle k, (b) the filter inductance L, (c) the filter capacitor C, and (d) the critical values of L and C.

Solution

$V_s = 12\,\text{V}$, $\Delta V_c = 20\,\text{mV}$, $\Delta I - 0.8\,\text{A}$, $f = 25\,\text{kHz}$, and $V_a = 5\,\text{V}$.

a. From Eq. (5.56), $V_a = kV_s$ and $k = V_a/V_s = 5/12 = 0.4167 = 41.67\%$.

b. From Eq. (5.59),

$$L = \frac{5(12-5)}{0.8 \times 25{,}000 \times 12} = 145.83\,\mu\text{H}$$

c. From Eq. (5.61),

$$C = \frac{0.8}{8 \times 20 \times 10^{-3} \times 25{,}000} = 200\,\mu\text{F}$$

d. From Eq. (5.64), we get $L_c = \dfrac{(1-k)R}{2f} = \dfrac{(1-0.4167)\times 500}{2\times 25\times 10^3} = 5.83\,\text{mH}$

From Eq. (5.65), we get $C_c = \dfrac{1-k}{16Lf^2} = \dfrac{1-0.4167}{16\times 145.83\times 10^{-6}\times (25\times 10^3)^2} = 0.4\,\mu\text{F}$

5.9.2 Boost Regulators

In a boost regulator [8, 9] the output voltage is greater than the input voltage—hence the name "boost." A boost regulator using a power MOSFET is shown in Figure 5.18a. Transistor M_1 acts as a controlled switch and diode D_m is an uncontrolled switch. The circuit in Figure 5.18a is often represented by two switches as shown in Figure 5.18b. The circuit operation can be divided into two modes. Mode 1 begins when transistor. M_1 is switched on at $t = 0$. The input current, which rises, flows through inductor L and transistor Q_1. Mode 2 begins when transistor M_1 is switched off at $t = t_1$. The current that was flowing through the transistor would now flow through L, C, load, and diode D_m. The inductor current falls until transistor M_1 is turned on again in the next cycle. The energy stored in inductor L is transferred to the load. The equivalent circuits for the modes of operation are shown in Figure 5.18c. The waveforms for voltages and currents are shown in Figure 5.18d for continuous load current, assuming that the current rises or falls linearly.

Assuming that the inductor current rises linearly from I_1 to I_2 in time t_1,

$$V_s = L\frac{I_2 - I_1}{t_1} = L\frac{\Delta I}{t_1} \tag{5.66}$$

or

$$t_1 = \frac{\Delta IL}{V_s} \tag{5.67}$$

and the inductor current falls linearly from I_2 to I_1 in time t_2,

$$V_s - V_a = -L\frac{\Delta I}{t_2} \tag{5.68}$$

or

$$t_2 = \frac{\Delta IL}{V_a - V_s} \tag{5.69}$$

where $\Delta I = I_2 - I_1$ is the peak-to-peak ripple current of inductor L. From Eqs. (5.66) and (5.68),

$$\Delta I = \frac{V_s t_1}{L} = \frac{(V_a - V_s)t_2}{L}$$

Substituting $t_1 = kT$ and $t_2 = (1-k)T$ yields the average output voltage,

$$V_a = V_s\frac{T}{t_2} = \frac{V_s}{1-k} \tag{5.70}$$

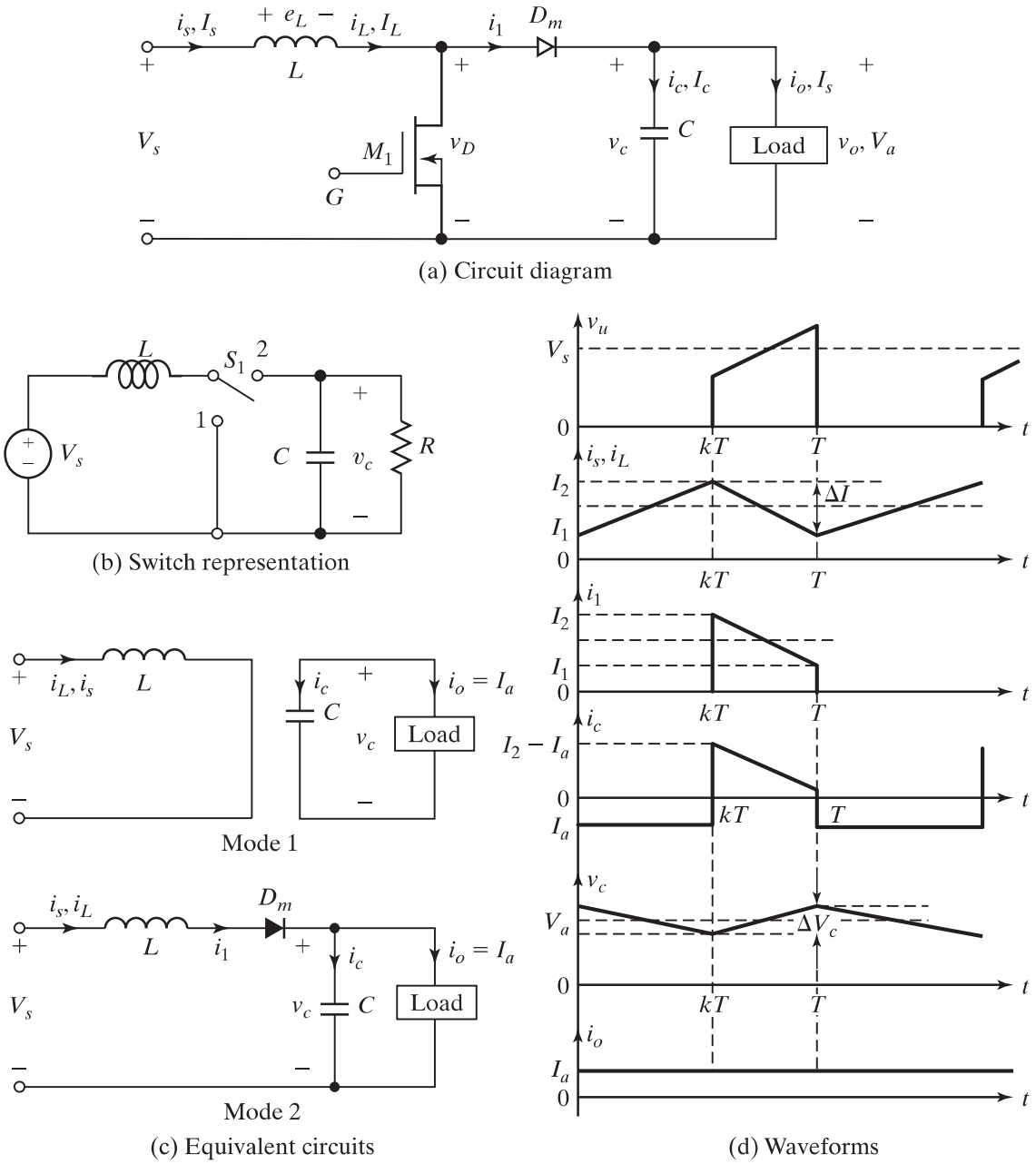


FIGURE 5.18

Boost regulator with continuous i_L.

which gives

$$(1 - k) = \frac{V_s}{V_a} \tag{5.71}$$

Substituting $k = t_1/T = t_1 f$ into Eq. (5.71) yields

$$t_1 = \frac{V_a - V_s}{V_a f} \tag{5.72}$$

Assuming a lossless circuit, $V_s I_s = V_a I_a = V_s I_a/(1 - k)$ and the average input current is

$$I_s = \frac{I_a}{1 - k} \tag{5.73}$$

Peak-to-peak inductor ripple current. The switching period T can be found from

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta IL}{V_s} + \frac{\Delta IL}{V_a - V_s} = \frac{\Delta ILV_a}{V_s(V_a - V_s)} \tag{5.74}$$

and this gives the peak-to-peak ripple current:

$$\Delta I = \frac{V_s(V_a - V_s)}{fLV_a} \tag{5.75}$$

or

$$\Delta I = \frac{V_s k}{fL} \tag{5.76}$$

Peak-to-peak capacitor ripple voltage. When the transistor is on, the capacitor supplies the load current for $t = t_1$. The average capacitor current during time t_1 is $I_c = I_a$ and the peak-to-peak ripple voltage of the capacitor is

$$\Delta V_c = v_c - v_c(t = 0) = \frac{1}{C}\int_0^{t_1} I_c\, dt = \frac{1}{C}\int_0^{t_1} I_a\, dt = \frac{I_a t_1}{C} \tag{5.77}$$

Substituting $t_1 = (V_a - V_s)/(V_a f)$ from Eq. (5.72) gives

$$\Delta V_c = \frac{I_a(V_a - V_s)}{V_a fC} \tag{5.78}$$

or

$$\Delta V_c = \frac{I_a k}{fC} \tag{5.79}$$

Condition for continuous inductor current and capacitor voltage. If I_L is the average inductor current, at the critical condition for continuous conduction the inductor ripple current $\Delta I = 2I_L$.

Using Eqs. (5.70) and (5.76), we get

$$\frac{kV_s}{fL} = 2I_L = 2I_s = \frac{2V_s}{(1 - k)^2}$$

which gives the critical value of the inductor L_c as

$$L_c = L = \frac{k(1 - k)R}{2f} \tag{5.80}$$

If V_c is the average capacitor voltage, at the critical condition for continuous conduction the capacitor ripple voltage $\Delta V_c = 2V_a$. Using Eq. (5.79), we get

$$\frac{I_a k}{Cf} = 2V_a = 2I_a R$$

which gives the critical value of the capacitor C_c as

$$C_c = C = \frac{k}{2fR} \tag{5.81}$$

A boost regulator can step up the output voltage without a transformer. Due to a single transistor, it has a high efficiency. The input current is continuous. However, a high-peak current has to flow through the power transistor. The output voltage is very sensitive to changes in duty cycle k and it might be difficult to stabilize the regulator. The average output current is less than the average inductor current by a factor of $(1 - k)$, and a much higher rms current would flow through the filter capacitor, resulting in the use of a larger filter capacitor and a larger inductor than those of a buck regulator.

Example 5.6 Finding the Currents and Voltage in the Boost Regulator

A boost regulator in Figure 5.18a has an input voltage of $V_s = 5\,\text{V}$. The average output voltage $V_a = 15\,\text{V}$ and the average load current $I_a = 0.5\,\text{A}$. The switching frequency is 25 kHz. If $L = 150\,\mu\text{H}$ and $C = 220\,\mu\text{F}$, determine (a) the duty cycle k, (b) the ripple current of inductor ΔI, (c) the peak current of inductor I_2, (d) the ripple voltage of filter capacitor ΔV_c, and (e) the critical values of L and C.

Solution

$V_s = 5\,\text{V}, V_a = 15\,\text{V}, f = 25\,\text{kHz}, L = 150\,\mu\text{H}$, and $C = 220\,\mu\text{F}$.

a. From Eq. (5.70), $15 = 5/(1 - k)$ or $k = 2/3 = 0.6667 = 66.67\%$.

b. From Eq. (5.75),

$$\Delta I = \frac{5 \times (15 - 5)}{25{,}000 \times 150 \times 10^{-6} \times 15} = 0.89\,\text{A}$$

c. From Eq. (5.73), $I_s = 0.5/(1 - 0.667) = 1.5\,\text{A}$ and peak inductor current,

$$I_2 = I_s + \frac{\Delta I}{2} = 1.5 + \frac{0.89}{2} = 1.945\,\text{A}$$

d. From Eq. (5.79),

$$\Delta V_c = \frac{0.5 \times 0.6667}{25{,}000 \times 220 \times 10^{-6}} = 60.61\,\text{mV}$$

e. $R = \dfrac{V_a}{I_a} = \dfrac{15}{0.5} = 30\,\Omega$

From Eq. (5.80), we get $L_c = \dfrac{(1-k)kR}{2f} = \dfrac{(1-0.6667)\times 0.6667\times 30}{2\times 25\times 10^3} = 133\,\mu\text{H}$

From Eq. (5.81), we get $C_c = \dfrac{k}{2fR} = \dfrac{0.6667}{2\times 25\times 10^3\times 30} = 0.44\,\mu\text{F}$

5.9.3 Buck–Boost Regulators

A buck–boost regulator provides an output voltage that may be less than or greater than the input voltage—hence the name "buck–boost"; the output voltage polarity is opposite to that of the input voltage. This regulator is also known as an *inverting regulator*. The circuit arrangement of a buck–boost regulator is shown in Figure 5.19a. Transistor Q_1 acts as a controlled switch and diode D_m is an uncontrolled switch. They operate as two SPST current-bidirectional switches. The circuit in Figure 5.19a is often represented by two switches as shown in Figure 5.19b.

The circuit operation can be divided into two modes. During mode 1, transistor Q_1 is turned on and diode D_m is reversed biased. The input current, which rises, flows through inductor L and transistor Q_1. During mode 2, transistor Q_1 is switched off and the current, which was flowing through inductor L, would flow through L, C, D_m, and the load. The energy stored in inductor L would be transferred to the load and the inductor current would fall until transistor Q_1 is switched on again in the next cycle. The equivalent circuits for the modes are shown in Figure 5.19c. The waveforms for steady-state voltages and currents of the buck–boost regulator are shown in Figure 5.19d for a continuous load current.

Assuming that the inductor current rises linearly from I_1 to I_2 in time t_1,

$$V_s = L\frac{I_2 - I_1}{t_1} = L\frac{\Delta I}{t_1} \tag{5.82}$$

or

$$t_1 = \frac{\Delta I L}{V_s} \tag{5.83}$$

and the inductor current falls linearly from I_2 to I_1 in time t_2,

$$V_a = -L\frac{\Delta I}{t_2} \tag{5.84}$$

or

$$t_2 = \frac{-\Delta I L}{V_a} \tag{5.85}$$

where $\Delta I = I_2 - I_1$ is the peak-to-peak ripple current of inductor L. From Eqs. (5.82) and (5.84),

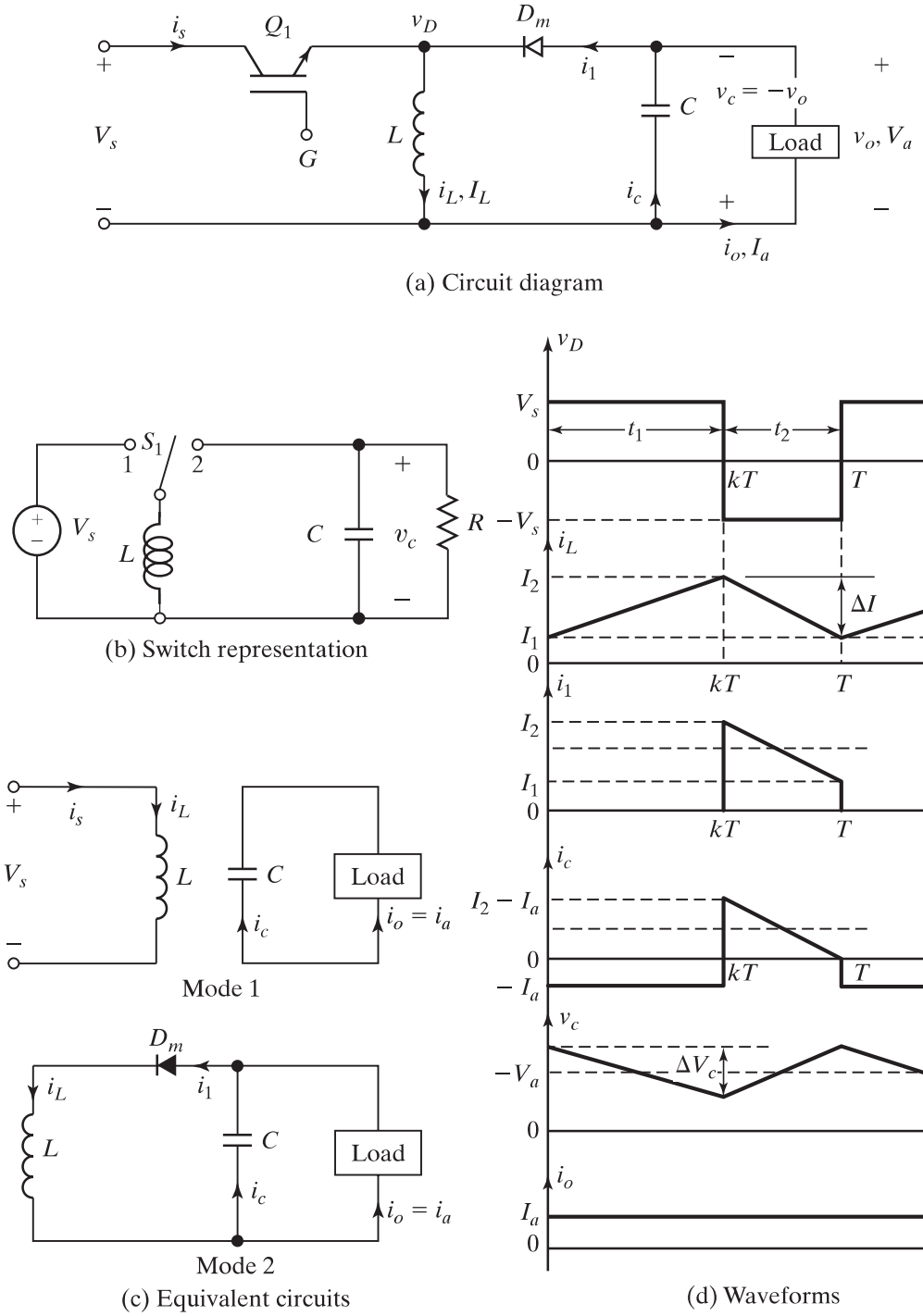


FIGURE 5.19

Buck–boost regulator with continuous i_L.

$$\Delta I = \frac{V_s t_1}{L} = \frac{-V_a t_2}{L}$$

Substituting $t_1 = kT$ and $t_2 = (1 - k)T$, the average output voltage is

$$V_a = -\frac{V_s k}{1 - k} \tag{5.86}$$

Substituting $t_1 = kT$ and $t_2 = (1 - k)T$ into Eq. (5.86) yields

$$(1 - k) = \frac{-V_s}{V_a - V_s} \tag{5.87}$$

Substituting $t_2 = (1 - k)T$, and $(1 - k)$ from Eq. (5.87) into Eq. (5.86) yields

$$t_1 = \frac{V_a}{(V_a - V_s)f} \tag{5.88}$$

Assuming a lossless circuit, $V_s I_s = -V_a I_a = V_s I_a k/(1 - k)$ and the average input current I_s is related to the average output current I_a by

$$I_s = \frac{I_a k}{1 - k} \tag{5.89}$$

Peak-to-peak inductor ripple current. The switching period T can be found from

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta IL}{V_s} - \frac{\Delta IL}{V_a} = \frac{\Delta IL(V_a - V_s)}{V_s V_a} \tag{5.90}$$

and this gives the peak-to-peak ripple current,

$$\Delta I = \frac{V_s V_a}{fL(V_a - V_s)} \tag{5.91}$$

or

$$\Delta I = \frac{V_s k}{fL} \tag{5.92}$$

The average inductor current is given by

$$I_L = I_s + I_a = \frac{kI_a}{1 - k} + I_a = \frac{I_a}{1 - k} \tag{5.92a}$$

Peak-to-peak capacitor ripple voltage. When transistor Q_1 is on, the filter capacitor supplies the load current for $t = t_1$. The average discharging current of the capacitor is $I_c = -I_a$ and the peak-to-peak ripple voltage of the capacitor is

$$\Delta V_c = \frac{1}{C}\int_0^{t_1} -I_c\, dt = \frac{1}{C}\int_0^{t_1} I_a\, dt = \frac{I_a t_1}{C} \tag{5.93}$$

Substituting $t_1 = V_a/[(V_a - V_s)f]$ from Eq. (5.88) becomes

$$\Delta V_c = \frac{I_a V_a}{(V_a - V_s)fC} \tag{5.94}$$

or

$$\Delta V_c = \frac{I_a k}{fC} \tag{5.95}$$

Condition for continuous inductor current and capacitor voltage. If I_L is the average inductor current, at the critical condition for continuous conduction the inductor ripple current $\Delta I = 2I_L$. Using Eqs. (5.86) and (5.92), we get

$$\frac{kV_s}{fL} = 2I_L = 2I_a = \frac{2kV_s}{(1-k)R}$$

which gives the critical value of the inductor L_c as

$$L_c = L = \frac{(1-k)R}{2f} \tag{5.96}$$

If V_c is the average capacitor voltage, at the critical condition for continuous conduction the capacitor ripple voltage $\Delta V_c = -2V_a$. Using Eq. (5.95), we get

$$-\frac{I_a k}{Cf} = -2V_a = -2I_a R$$

which gives the critical value of the capacitor C_c as

$$C_c = C = \frac{k}{2fR} \tag{5.97}$$

A buck–boost regulator provides output voltage polarity reversal without a transformer. It has high efficiency. Under a fault condition of the transistor, the *di/dt* of the fault current is limited by the inductor L and will be V_s/L. Output short-circuit protection would be easy to implement. However, the input current is discontinuous and a high peak current flows through transistor Q_1.

Example 5.7 Finding the Currents and Voltage in the Buck–Boost Regulator

The buck–boost regulator in Figure 5.19a has an input voltage of $V_s = 12\,\text{V}$. The duty cycle $k = 0.25$ and the switching frequency is 25 kHz. The inductance $L = 150\,\mu\text{H}$ and filter capacitance $C = 220\,\mu\text{F}$. The average load current $I_a = 1.25\,\text{A}$. Determine (a) the average output voltage, V_a; (b) the peak-to-peak output voltage ripple, ΔV_c; (c) the peak-to-peak ripple current of inductor, ΔI; (d) the peak current of the transistor, I_p; and (e) the critical values of L and C.

Solution

$V_s = 12\,\text{V}, k = 0.25, I_a = 1.25\,\text{A}, f = 25\,\text{kHz}, L = 150\,\mu\text{H}$, and $C = 220\,\mu\text{F}$.

a. From Eq. (5.86), $V_a = -12 \times 0.25/(1 - 0.25) = -4\,\text{V}$.

b. From Eq. (5.95), the peak-to-peak output ripple voltage is

$$\Delta V_c = \frac{1.25 \times 0.25}{25{,}000 \times 220 \times 10^{-6}} = 56.8\,\text{mV}$$

c. From Eq. (5.92), the peak-to-peak inductor ripple is

$$\Delta I = \frac{12 \times 0.25}{25{,}000 \times 150 \times 10^{-6}} = 0.8\,\text{A}$$

d. From Eq. (5.89), $I_s = 1.25 \times 0.25/(1 - 0.25) = 0.4167\,\text{A}$. Because I_s is the average of duration kT, the peak-to-peak current of the transistor,

$$I_p = \frac{I_s}{k} + \frac{\Delta I}{2} = \frac{0.4167}{0.25} + \frac{0.8}{2} = 2.067\,\text{A}$$

e. $R = \dfrac{-V_a}{I_a} = \dfrac{4}{1.25} = 3.2\,\Omega$

From Eq. (5.96), we get $L_c = \dfrac{(1-k)R}{2f} = \dfrac{(1 - 0.25) \times 3.2}{2 \times 25 \times 10^3} = 450\,\mu\text{H}.$

From Eq. (5.97), we get $C_c = \dfrac{k}{2fR} = \dfrac{0.25}{2 \times 25 \times 10^3 \times 3.2} = 1.56\,\mu\text{F}.$

5.9.4 Cúk Regulators

The circuit arrangement of the Cúk regulator [10] using a power bipolar junction transistor is shown in Figure 5.20a. Similar to the buck–boost regulator, the Cúk regulator provides an output voltage that is less than or greater than the input voltage, but the output voltage polarity is opposite to that of the input voltage. It is named after its inventor [1]. When the input voltage is turned on and transistor Q_1 is switched off, diode D_m is forward biased and capacitor C_1 is charged through L_1, D_m, and the input supply V_s. Transistor Q_1 acts a controlled switch and diode D_m is an uncontrolled switch. They operate as two SPST current-bidirectional switches. The circuit in Figure 5.20a is often represented by two switches as shown in Figure 5.20b.

The circuit operation can be divided into two modes. Mode 1 begins when transistor Q_1 is turned on at $t = 0$. The current through inductor L_1 rises. At the same time, the voltage of capacitor C_1 reverse biases diode D_m and turns it off. The capacitor C_1 discharges its energy to the circuit formed by C_1, C_2, the load, and L_2. Mode 2 begins when transistor Q_1 is turned off at $t = t_1$. The capacitor C_1 is charged from the input supply and the energy stored in the inductor L_2 is transferred to the load. The diode D_m and transistor Q_1 provide a synchronous switching action. The capacitor C_1 is the medium for transferring energy from the source to the load. The equivalent circuits for the modes are shown in Figure 5.20c and the waveforms for steady-state voltages and currents are shown in Figure 5.20d for a continuous load current.

Assuming that the current of inductor L_1 rises linearly from I_{L11} to I_{L12} in time t_1,

$$V_s = L_1 \frac{I_{L12} - I_{L11}}{t_1} = L_1 \frac{\Delta I_1}{t_1} \tag{5.98}$$

or

$$t_1 = \frac{\Delta I_1 L_1}{V_s} \tag{5.99}$$

and due to the charged capacitor C_1, the current of inductor L_1 falls linearly from I_{L12} to I_{L11} in time t_2,

$$V_s - V_{c1} = -L_1 \frac{\Delta I_1}{t_2} \tag{5.100}$$

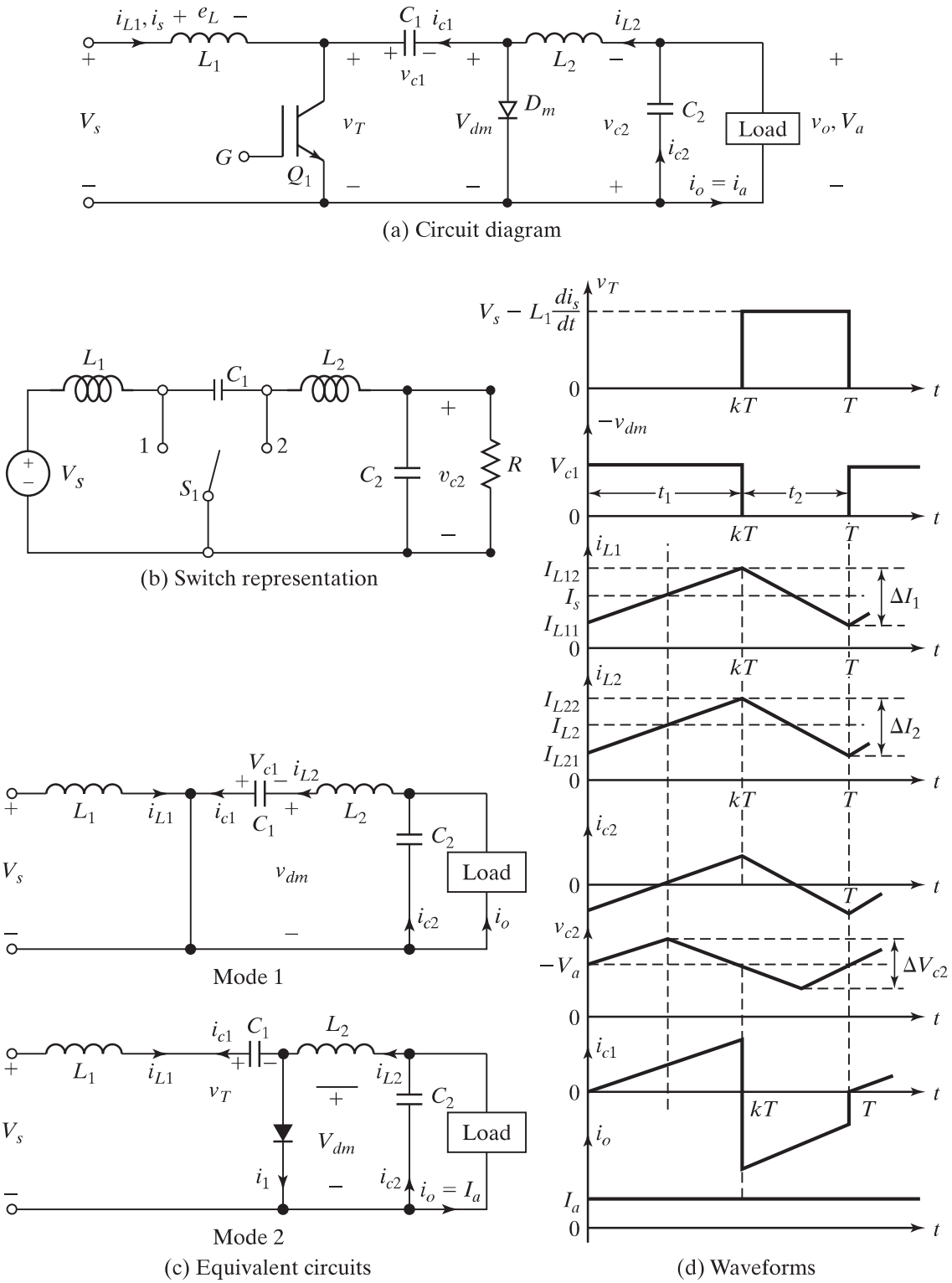


FIGURE 5.20

Cúk regulator.

or

$$t_2 = \frac{-\Delta I_1 L_1}{V_s - V_{c1}} \tag{5.101}$$

where V_{c1} is the average voltage of capacitor C_1, and $\Delta I_1 = I_{L12} - I_{L11}$. From Eqs. (5.98) and (5.100).

$$\Delta I_1 = \frac{V_s t_1}{L_1} = \frac{-(V_s - V_{c1})t_2}{L_1}$$

Substituting $t_1 = kT$ and $t_2 = (1 - k)T$, the average voltage of capacitor C_1 is

$$V_{c1} = \frac{V_s}{1 - k} \tag{5.102}$$

Assuming that the current of filter inductor L_2 rises linearly from I_{L21} to I_{L22} in time t_1,

$$V_{c1} + V_a = L_2 \frac{I_{L22} - I_{L21}}{t_1} = L_2 \frac{\Delta I_2}{t_1} \tag{5.103}$$

or

$$t_1 = \frac{\Delta I_2 L_2}{V_{c1} + V_a} \tag{5.104}$$

and the current of inductor L_2 falls linearly from I_{L22} to I_{L21} in time t_2,

$$V_a = -L_2 \frac{\Delta I_2}{t_2} \tag{5.105}$$

or

$$t_2 = -\frac{\Delta I_2 L_2}{V_a} \tag{5.106}$$

where $\Delta I_2 = I_{L22} - I_{L21}$. From Eqs. (5.103) and (5.105),

$$\Delta I_2 = \frac{(V_{c1} + V_a)t_1}{L_2} = -\frac{V_a t_2}{L_2}$$

Substituting $t_1 = kT$ and $t_2 = (1 - k)T$, the average voltage of capacitor C_1 is

$$V_{c1} = -\frac{V_a}{k} \tag{5.107}$$

Equating Eq. (5.102) to Eq. (5.107), we can find the average output voltage as

$$V_a = -\frac{kV_s}{1 - k} \tag{5.108}$$

which gives

$$k = \frac{V_a}{V_a - V_s} \tag{5.109}$$

$$1 - k = \frac{V_s}{V_s - V_a} \tag{5.110}$$

Assuming a lossless circuit, $V_s I_s = -V_a I_a = V_s I_a k/(1 - k)$ and the average input current,

$$I_s = \frac{kI_a}{1 - k} \tag{5.111}$$

Peak-to-peak ripple currents of inductors. The switching period T can be found from Eqs. (5.99) and (5.101):

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta I_1 L_1}{V_s} - \frac{\Delta I_1 L_1}{V_s - V_{c1}} = \frac{-\Delta I_1 L_1 V_{c1}}{V_s(V_s - V_{c1})} \tag{5.112}$$

which gives the peak-to-peak ripple current of inductor L_1 as

$$\Delta I_1 = \frac{-V_s(V_s - V_{c1})}{fL_1 V_{c1}} \tag{5.113}$$

or

$$\Delta I_1 = \frac{V_s k}{fL_1} \tag{5.114}$$

The switching period T can also be found from Eqs. (5.104) and (5.106):

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta I_2 L_2}{V_{c1} + V_a} - \frac{\Delta I_2 L_2}{V_a} = \frac{-\Delta I_2 L_2 V_{c1}}{V_a(V_{c1} + V_a)} \tag{5.115}$$

and this gives the peak-to-peak ripple current of inductor L_2 as

$$\Delta I_2 = \frac{-V_a(V_{c1} + V_a)}{fL_2 V_{c1}} \tag{5.116}$$

or

$$\Delta I_2 = -\frac{V_a(1 - k)}{fL_2} = \frac{kV_s}{fL_2} \tag{5.117}$$

Peak-to-peak ripple voltages of capacitors. When transistor Q_1 is off, the energy transfer capacitor C_1 is charged by the input current for time $t = t_2$. The average charging current for C_1 is $I_{c1} = I_s$ and the peak-to-peak ripple voltage of the capacitor C_1 is

$$\Delta V_{c1} = \frac{1}{C_1}\int_0^{t_2} I_{c1}\, dt = \frac{1}{C_1}\int_0^{t_2} I_s\, dt = \frac{I_s t_2}{C_1} \tag{5.118}$$

Equation (5.110) gives $t_2 = V_s/[(V_s - V_a)f]$ and Eq. (5.118) becomes

$$\Delta V_{c1} = \frac{I_s V_s}{(V_s - V_a)fC_1} \tag{5.119}$$

or

$$\Delta V_{c1} = \frac{I_s(1-k)}{fC_1} \tag{5.120}$$

If we assume that the load current ripple Δi_o is negligible, $\Delta i_{L2} = \Delta i_{c2}$. The average charging current of C_2, which flows for time $T/2$, is $I_{c2} = \Delta I_2/4$ and the peak-to-peak ripple voltage of capacitor C_2 is

$$\Delta V_{c2} = \frac{1}{C_2}\int_0^{T/2} I_{c2}\,dt = \frac{1}{C_2}\int_0^{T/2}\frac{\Delta I_2}{4}\,dt = \frac{\Delta I_2}{8fC_2} \tag{5.121}$$

or

$$\Delta V_{c2} = \frac{V_a(1-k)}{8C_2L_2f^2} = \frac{kV_s}{8C_2L_2f^2} \tag{5.122}$$

Condition for continuous inductor current and capacitor voltage. If I_{L1} is the average current of inductor L_1, the inductor ripple current $\Delta I_1 = 2I_{L1}$. Using Eqs. (5.111) and (5.114), we get

$$\frac{kV_S}{fL_1} = 2I_{L1} = 2I_S = \frac{2kI_a}{1-k} = 2\left(\frac{k}{1-k}\right)^2\frac{V_S}{R}$$

which gives the critical value of the inductor L_{c1} as

$$L_{c1} = L_1 = \frac{(1-k)^2R}{2kf} \tag{5.123}$$

If I_{L2} is the average current of inductor L_2, the inductor ripple current $\Delta I_2 - 2I_{L2}$. Using Eqs. (5.108) and (5.117), we get

$$\frac{kV_S}{fL_2} = 2I_{L2} = 2I_a = \frac{2V_a}{R} = \frac{2kV_S}{(1-k)R}$$

which gives the critical value of the inductor L_{c2} as

$$L_{c2} = L_2 = \frac{(1-k)R}{2f} \tag{5.124}$$

If V_{c1} is the average capacitor voltage, the capacitor ripple voltage $\Delta V_{c1} = 2V_a$. Using $\Delta V_{c1} = 2V_a$ into Eq. (5.120), we get

$$\frac{I_S(1-k)}{fC_1} = 2V_a = 2I_aR$$

which, after substituting for I_S, gives the critical value of the capacitor C_{c1} as

$$C_{c1} = C_1 = \frac{k}{2fR} \tag{5.125}$$

If V_{c2} is the average capacitor voltage, the capacitor ripple voltage $\Delta V_{c2} = 2V_a$. Using Eq. (5.108) and (5.122), we get

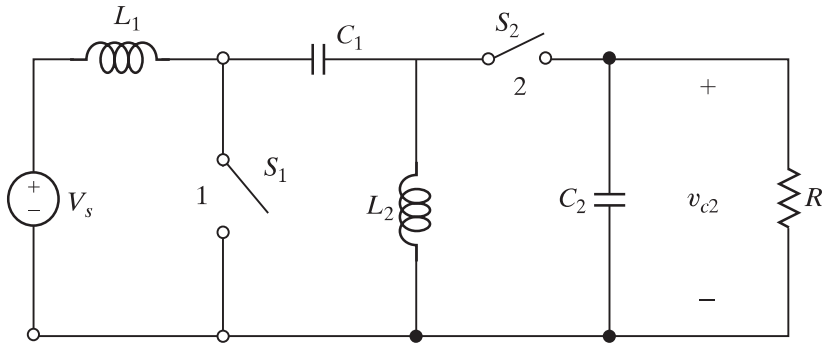
$$\frac{kV_S}{8C_2L_2f^2} = 2V_a = \frac{2kV_S}{1-k}$$

which, after substituting for L_2 from Eq. (5.124), gives the critical value of the capacitor C_{c2} as

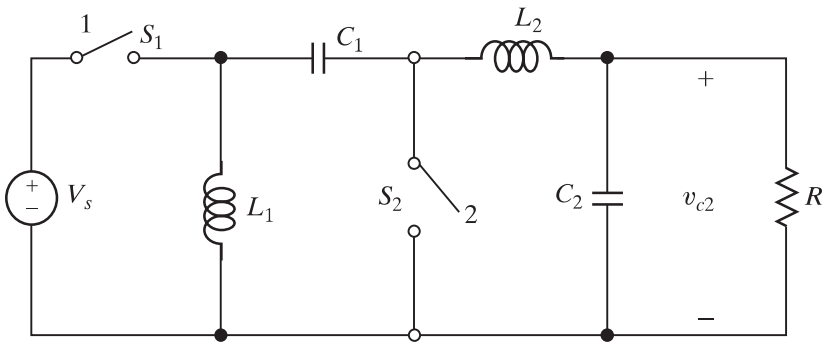
$$C_{c2} = C_2 = \frac{1}{8fR} \tag{5.126}$$

The Cúk regulator is based on the capacitor energy transfer. As a result, the input current is continuous. The circuit has low switching losses and has high efficiency. When transistor Q_1 is turned on, it has to carry the currents of inductors L_1 and L_2. As a result a high peak current flows through transistor Q_1. Because the capacitor provides the energy transfer, the ripple current of the capacitor C_1 is also high. This circuit also requires an additional capacitor and inductor.

The Cúk converter, which has an inverting buck–boost characteristic, exhibits nonpulsating input and output terminal currents. The single-ended primary inductance converter (SEPIC), which is a noninverting Cúk converter, can be formed by interchanging the locations of diode D_m and inductor L_2 in Figure 5-20a. The SEPIC [35] is shown in Figure 5.21a. The Cúk and SEPIC also exhibit a desirable feature such that the switching MOSFET's source terminal is connected directly to the common ground. This simplifies the construction of the gate-drive circuitry. The output voltage of both



(a) SEPIC



(b) Inverse of SEPIC

FIGURE 5.21
SEPIC converter.

SEPIC and its inverse is $V_a = V_S k/(1-k)$. The inverse of SEPIC is formed by interchanging the locations of the switches and the inductors as shown in Figure 5.21b.

Example 5.8 Finding the Currents and Voltages in the Cúk Regulator

The input voltage of a Cúk converter in Figure 5.20a is $V_s = 12\,\text{V}$. The duty cycle is $k = 0.25$ and the switching frequency is 25 kHz. The filter inductance is $L_2 = 150\,\mu\text{H}$ and filter capacitance is $C_2 = 220\,\mu\text{F}$. The energy transfer capacitance is $C_1 = 200\,\mu\text{F}$ and inductance $L_1 = 180\,\mu\text{H}$. The average load current is $I_a = 1.25\,\text{A}$. Determine (a) the average output voltage V_a; (b) the average input current I_s; (c) the peak-to-peak ripple current of inductor L_1, ΔI_1; (d) the peak-to-peak ripple voltage of capacitor C_1, ΔV_{c1}; (e) the peak-to-peak ripple current of inductor L_2, ΔI_2; (f) the peak-to-peak ripple voltage of capacitor C_2, ΔV_{c2}; and (g) the peak current of the transistor I_p.

Solution

$V_s = 12\,\text{V}$, $k = 0.25$, $I_a = 1.25\,\text{A}$, $f = 25\,\text{kHz}$, $L_1 = 180\,\mu\text{H}$, $C_1 = 200\,\mu\text{F}$, $L_2 = 150\,\mu\text{H}$, and $C_2 = 220\,\mu\text{F}$.

a. From Eq. (5.108), $V_a = -0.25 \times 12/(1-0.25) = -4\,\text{V}$.

b. From Eq. (5.111), $I_s = 1.25 \times 0.25/(1-0.25) = 0.42\,\text{A}$.

c. From Eq. (5.114), $\Delta I_1 = 12 \times 0.25/(25{,}000 \times 180 \times 10^{-6}) = 0.67\,\text{A}$.

d. From Eq. (5.120), $\Delta V_{c1} = 0.42 \times (1-0.25)/(25{,}000 \times 200 \times 10^{-6}) = 63\,\text{mV}$.

e. From Eq. (5.117), $\Delta I_2 = 0.25 \times 12/(25{,}000 \times 150 \times 10^{-6}) = 0.8\,\text{A}$.

f. From Eq. (5.121), $\Delta V_{c2} = 0.8/(8 \times 25{,}000 \times 220 \times 10^{-6}) = 18.18\,\text{mV}$.

g. The average voltage across the diode can be found from

$$V_{dm} = -kV_{c1} = -V_a k\frac{1}{-k} = V_a \tag{5.127}$$

For a lossless circuit, $I_{L2}V_{dm} = V_a I_a$ and the average value of the current in inductor L_2 is

$$\begin{aligned} I_{L2} &= \frac{I_a V_a}{V_{dm}} = I_a \\ &= 1.25\,\text{A} \end{aligned} \tag{5.128}$$

Therefore, the peak current of transistor is

$$I_p = I_s + \frac{\Delta I_1}{2} + I_{L2} + \frac{\Delta I_2}{2} = 0.42 + \frac{0.67}{2} + 1.25 + \frac{0.8}{2} = 2.405\,\text{A}$$

5.9.5 Limitations of Single-Stage Conversion

The four regulators use only one transistor, employing only one stage conversion, and require inductors or capacitors for energy transfer. Due to the current-handling limitation of a single transistor, the output power of these regulators is small, typically tens of watts. At a higher current, the size of these components increases, with increased component losses, and the efficiency decreases. In addition, there is no isolation between the input and output voltage, which is a highly desirable criterion in most applications. For high-power applications, multistage conversions are used,

where a dc voltage is converted to ac by an inverter. The ac output is isolated by a transformer and then converted to dc by rectifiers. The multistage conversions are discussed in Section 13-4.

Key Points of Section 5.9

- A dc regulator can produce a dc output voltage, which is higher or lower than the dc supply voltage. *LC* filters are used to reduce the ripple content of the output voltage. Depending on the type of the regulator, the polarity of the output voltage can be opposite of the input voltage.

5.10 COMPARISON OF REGULATORS

When a current flows through an inductor, a magnetic field is set up. Any change in this current changes this field and an emf is induced. This emf acts in such a direction as to maintain the flux at its original density. This effect is known as the *self-induction*. An inductor limits the rise and fall of its currents and tries to maintain the ripple current low.

There is no change in the position of the main switch Q_1 for the buck and buck–boost regulators. Switch Q_1 is connected to the dc supply line. Similarly, there is no change in the position of the main switch Q_1 for the boost and Cúk regulators. Switch Q_1 is connected between the two supply lines. When the switch is closed, the supply is shorted through an inductor L, which limits the rate of rise of the supply current.

In Section 5.9, we derive the voltage gain of the regulators with the assumptions that there were no resistances associated with the inductors and capacitors. However, such resistances, though small, may reduce the gain significantly [11, 12]. Table 5.1 summarizes the voltage gains of the regulators. The comparisons of the voltage gains for different converters are shown in Figure 5.22. The output of the SEPIC is the inverse of the Cúk converter and has the features of the Cúk converter.

TABLE 5.1 Summaries of Regulator Gains [Ref. 11]

Regulator	Voltage Gain, $G(k) = V_a/V_S$ with Negligible Values of r_L and r_C	Voltage Gain, $G(k) = V_a/V_S$ with Finite Values of r_L and r_C
Buck	k	$\dfrac{kR}{R + r_L}$
Boost	$\dfrac{1}{1-k}$	$\dfrac{1}{1-k}\left[\dfrac{(1-k)^2R}{(1-k)^2R + r_L + k(1-k)\left(\dfrac{r_CR}{r_C+R}\right)}\right]$
Buck–boost	$\dfrac{-k}{1-k}$	$\dfrac{-k}{1-k}\left[\dfrac{(1-k)^2R}{(1-k)^2R + r_L + k(1-k)\left(\dfrac{r_CR}{r_C+R}\right)}\right]$

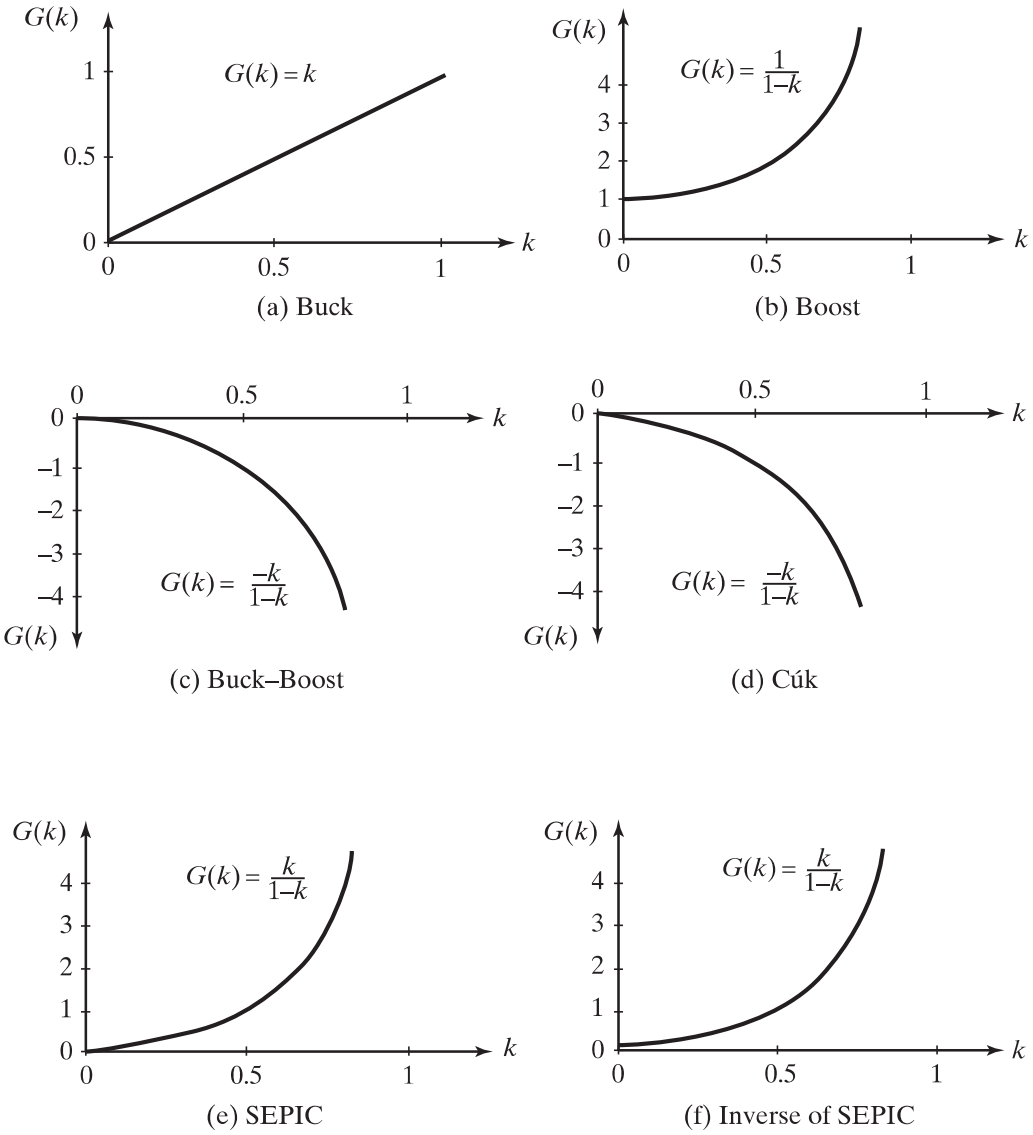


FIGURE 5.22

Comparison of converter voltage gains.

Inductors and capacitors act as energy storage elements in switched-mode regulators and as filter elements to smooth out the current harmonics. We can notice from Eqs. (B.17) and (B.18) in Appendix B that the magnetic loss increases with the square of frequency. On the other hand, a higher frequency reduces the size of inductors for the same value of ripple current and filtering requirement. The design of dc–dc converters requires a compromise among switching frequency, inductor sizes, capacitor sizes, and switching losses.

5.11 MULTIOUTPUT BOOST CONVERTER

For a digital signal processor, high-speed computation requires a high supply voltage V_s for fast switching. Because power consumption is proportional to the square of V_s, it is advisable to lower V_s when lower computation speed is needed [8, 9]. A boost converter

DC Power Supplies

Dr Suresh Kumar T

1

DC Power Supplies

PWM
(or)
Resonant Inverter
DC-AC

2-Stage Conv
F DC-AC
→ AC-DC

3-stage Cn
AC-DC
DC-AC
AC-DC

2

1 Switched mode Power Supply
2 Resonant Power Supply
3 Bidirectional Power Supply

3

Switched mode DC Power Supply

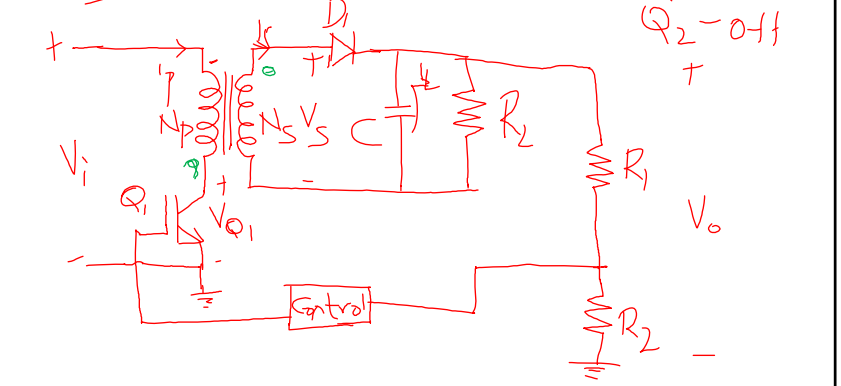
high η
high Current at low V

flyback forward
Push-pull
half Bridge
Full Bridge

Flyback
Forward Conv.

4

Fly back Converter



Q_1 - on
Q_2 - off

5

Q_1 - on

$0 < t \le kT$

duty cycle ratio.

$i_p = \frac{V_s t}{L_p}$ $\quad t = kT$ $\quad i_p$ reaches peak

$i_{p(pk)} = \frac{V_s kT}{L_p}$

6

$I_{sc(pk)} = \left(\frac{N_p}{N_s}\right) I_{p(pk)}$

mode 2 $\quad Q_1$ - off

$i_{sc} = I_{s(pk)} - \frac{V_o}{L_s} t$

7

i/p power

$P_i = \frac{\frac{1}{2} L_p I_{p(pk)}^2}{T} = \frac{(kV_s)^2}{2fL_p}$

η

$P_o = \eta P_i = \frac{\eta (kV_s)^2}{2fL_p}$

$V_s kT$

$P_o = \frac{V_o^2}{R_L}$ $\quad V_o = V_s k \sqrt{\frac{\eta R_L}{2fL_p}}$

8

$k_{max} \rightarrow V_{s(min)}$

$V_{s\,max}$.

$$k_{max} = \frac{V_o}{V_{s(min)}}\sqrt{\frac{2f_L}{\eta R_L}}$$

$$V_o = V_{s\,min}\, k_{max}\sqrt{\frac{\eta R_L}{2f_L}}$$

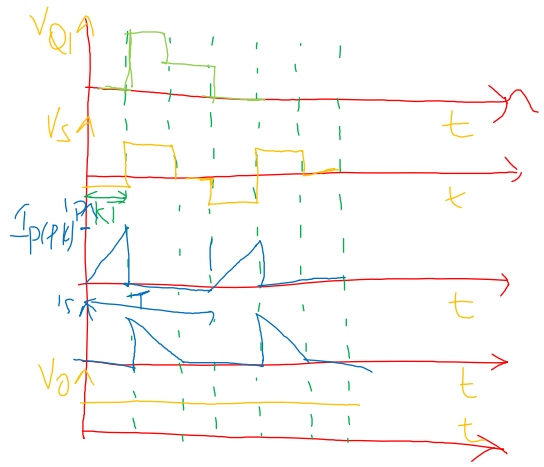
9

$$V_{R1(max)} = V_{s(max)} + \left(\frac{N_p}{N_s}\right) V_o$$

$$I_{c(max)} = I_{p(pk)} = \frac{2P_o}{\eta V_s}.$$

100W

10



11

12